READING MATERIAL FOR ANALOGUE &DIGITAL ELECTRONICS SUBJECT

2.4 ANALOGUE AND DIGITAL ELECTRONICS

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SYLLABUS

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Semiconductor devices

1.1 Concept of insulators, conductors and semi conductors, doping, minority and majority charge carriers.

1.2 P and N type semiconductors , PN junction diode, mechanism of current flow in PN junction, forward and reverse biased PN junction, potential barrier, drift and diffusion currents, depletion layer. V-I characteristics of diodes.

1.3 Concept of junction capacitance in forward and reverse biased condition. Characteristics and applications of Zener diodes . Zener and avalanche breakdown.

1.4 Diode as rectifier:-Diode as half-wave, full wave and bridge rectifiers. Peak Inverse Voltage, rectification efficiencies and ripple factor calculations, Concept of filters

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UNIT I: Semiconductor devices

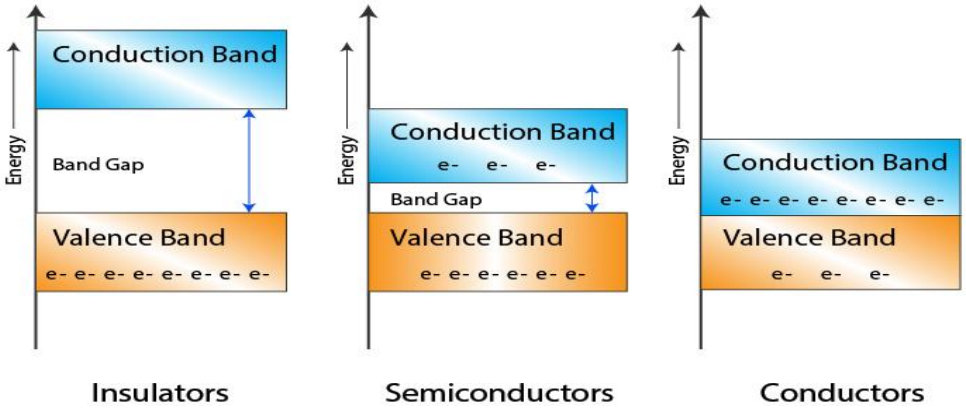
1.1 CONCEPT OF INSULATOR , CONDUCTOR AND SEMICONDUCTOR

Flow of electric current through a material depends upon the movement of charge carriers. These are free electrons which move in a solid in random directions. The property or conduction in a material depends upon the position of valence band, empty conduction band and the energy gap between them.

In a good conductor, the valence band and conduction bands overlap each other. Hence the free electrons require very little energy for their movement from valance band to conduction band. Current can easily flow through these metals.

Semiconductors have a small forbidden energy band. When energy is supplied in the form of heat or light, the valence electrons gain energy to cover the small forbidden energy band and become free to move in the structure of material. This allows flow of current through it. The conduction in semiconductor depends upon the free charge carriers which cross over to the conduction band. This depends upon the heat energy received by the electrons in valence band. Hence conductivity of a semiconductor depends upon its temperature. At higher temperature, more valance electrons will be able to move from valance band to conduction band. Thus flow of current will be easier at higher temperature. In silicon the forbidden energy band is 1.1 eV while in Germanium the forbidden energy band is 0.7 eV. The valence band is completely filled at 0K while conduction band is empty. Silicon and Germanium behave as perfect insulators at 0°k because there is no valance electron available for movement from valance band to conduction band.

Insulators have a large forbidden band. It may be around 10 eV. The electrons cannot cross over this band to reach the conduction band. The valence electrons are tightly bound to their parent atom. When a high energy is supplied, some electrons may be able to jump through the forbidden energy band thus constituting flow of a small current known as Leakage current. Increase in temperature increases energy of valence electrons and helps them to move to conduction band. Due to this reason the insulation resistance of insulators is reduced at higher temperatures. Fig.1 (a), (b) and (c) show the energy bands in insulators, semiconductors and conductors.



(a) Insulator (b)Semiconductor (c) Conductor

Fig.1.1 : Energy bands in materials

Materials are classified as conductors, Semiconductors and insulators on the basis of their resistivity . Resistivity is defined as the resistance to flow of electric current between opposite faces of a unit cube of that material.

Doping

The process of addition of impurity in an intrinsic semiconductor is called Doping.

Charge Carriers

Majority charge carriers and Minority charge carriers
The semiconductor has two types of charge carriers (i) free electrons (ii) holes

The process of doping creates conditions like $n_e > n_h$ or $n_h > n_e$ n-type and P-type semiconductors respectively. There is a concept of majority and minority carriers e.g in case of n-type semiconductor, $n_e > n_h$ thus the electrons are the majority carriers and hole are the minority carriers. Whenever there is a current flow through an extrinsic semiconductor, it is mainly due to flow of the majority charge carriers.

1.2 Types of semiconductors

Semiconductors

- Intrinsic (Pure Semiconductors)
- Extrinsic (Impure Semiconductors)

P-type N-type

There are two types of impurities that can be added to an intrinsic semiconductor.

(i) P-type impurity or Trivalent impurity
(ii) N-type impurity or Pentavalent impurity.

N type impurity: A material having 5 electrons in its valance orbit is known as an N type impurity. Examples of such impurities are:

Bismuth (Bi) Antimony (A) Arsenic (As) and Phosphorous (P).

Doping of an N-type impurity in an intrinsic semiconductor results in formation of N-type extrinsic Semiconductor. Such an impurity is Called DONOR impurity as it donates one free electron in the atomic structure of a semiconductors.

P-type impurity: A material having 3 electrons in its valence orbit is known as P-type impurity.

Examples of such impurities are

Gallium(G), Indium (In), Aluminum (Al) and Boron (B)

Doping of a P-type impurity n an intrinsic semiconductor results in formation of P-type extrinsic semiconductor. Such an impurity is called ACCEPTOR impurity as it accepts a free electron in the atomic structure of a semiconductor.

1.2.1 N-type Semiconductor

If a pentavalent material say phosphorous is doped to an intrinsic semiconductor it will result in formation of a N-type extrinsic semiconductor. An impurity atom is added to the structure of a silicon or Germanium atom. N-type semiconductor has

(1) Electron hole pairs generated due to thermal generation.

(2) Electrons donated by each atom of impurity atom.

1.2.2 P-type Semiconductor

When a small quantity of a trivalent impurity is doped to a pure crystal of semiconductor, a P-type semiconductor is formed.

P-type semiconductor has

(i) Electron hole pairs generated due to thermal generation.
(ii) Holes created by each atom of impurity atom.

1.2.3 P-N JUNCTION DIODE

It is a two terminal semiconductor device having the junction of a P-type semiconductor with N-type semiconductor on a Germanium or Silicon crystal. Thus a P-N junction is formed by joining a P-type material with a N-type material to have a regular crystal structure. In fact the P-N junction is formed by diffusing P-type material on one side and N-type material on the other side of a single crystal of Silicon or Germanium. P-type material joined with N-type material to form a P-N junction.Just after formation of the junction holes from P side will diffuse towards N sides and combine with the free electrons on N side. Similarly electrons from N side will diffuse towards P side and combine with majority of holes on P side. The PN junction is also known as a DIODE. It is represented by the symbol drawn in fig. . P side of diode is called ANODE and N side is called CATHODE denoted by A and K respectively. The symbolic representation of diode shown in fig 1.2.

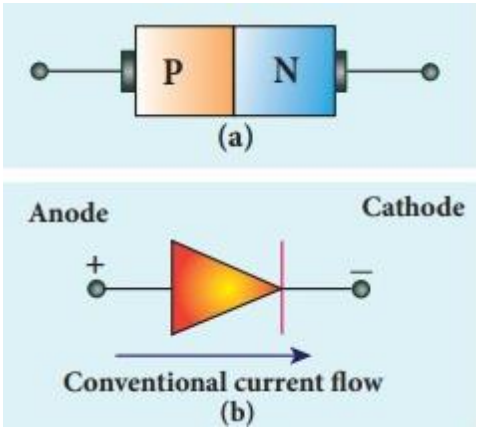


Fig.1.2 :Symbolic representation of a diode

This movement takes place due to difference in their concentration on two sides.

It would be expected that all holes of P side may diffuse to N side and all electrons on N side May diffuse to P side to combine with charges of opposite polarity, but it is not true. Diffusion of majority charge carriers (Holes on P-side and Electrons on N side) takes place near the junction only. This region near the junction in which combination of electrons and holes takes place is left with immobile ions only. P side near the junction has -ve ions while N side near the junction has +ve ions.

Positive ions on N side oppose further movement of holes from P side. Similarly negative ions on P side now oppose further flow of electrons from N side. Hence, restricting their movement across the junction. Movement of charge carriers is therefore stopped by the barrier formed near the junction due to charge on immobile ions.

1.2.4 Depletion layer or Region

A Small region near the junction is depleted of the mobile charge carriers due to combination of electrons and holes. This region has immobile ions only and is called DEPLETION REGION or DEPLETION LAYER.

The immobile ions in the depletion region have charge on them. (-ve charge on P side and +ve charge on N side). This sets up an electric field near the junction. This region is also termed as SPACE CHARGE REGION . The depletion region, and potential barrier are shown in fig 1.3

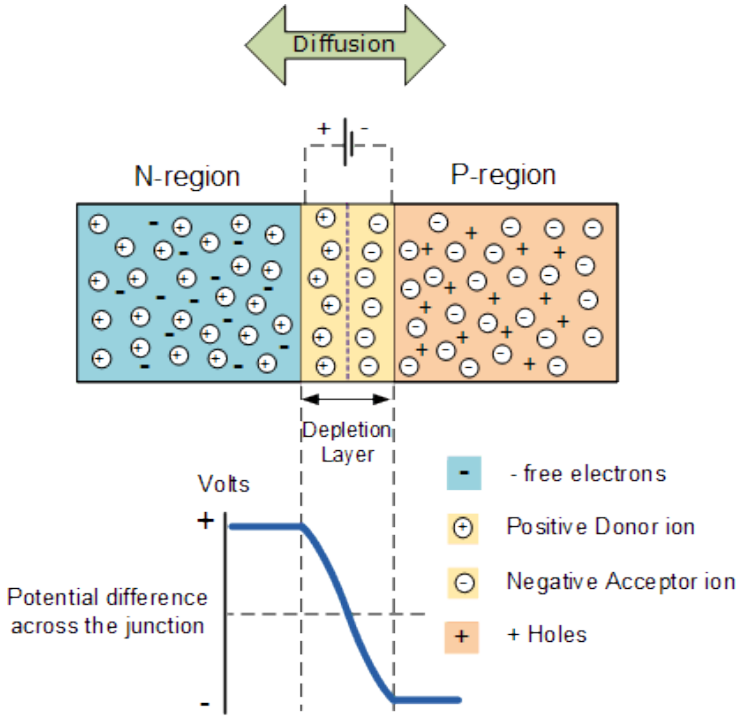


Fig.1.3:Deplition region and Potential barrier in PN Junction

1.2.5 Potential Barrier

Width of depletion region/space charge region or junction barrier is its physical distance from one side to the other side. Height of barrier is difference of Potential between two sides of barrier and is called Potential barrier. This potential barrier depends upon the semi conductor material used for formation of P-N junction. Its value is 0.7 V for Silicon and 0.3V for Germanium.

The potential barrier restricts the movement of majority carriers across the junction .The minority carriers (A few electrons on P side and a few holes on N side) are able to drift across the junction. Drift of these minority carries is balanced by diffusion of some of the high energy majority carriers. The potential barrier is formed in a P-N junction immediately on its formation.

1.2.6 Mechanism of current flow in PN junction

Biasing of PN Diode:-

A diode is said to be biased when it is connected to an external battery. A diode can be (i) Forward biased (ii) Reverse biased.

Forward biasing of Diode

A diode is said to be forward biased, if its anode is connected to +ve terminal of battery and its cathode is connected to -ve terminal of battery or power supply. In a forward biased diode, the width of potential barrier/depletion region is reduced. Electrons on N side of P-N diode are repelled by negative terminal of battery while holes on P side are repelled by positive terminal of battery. Both these majority carriers (Holes on P side and Electrons on N side) are able to cross over the junction due to energy gained by them by application of battery voltage.

Some of the majority carriers combine with opposite polarity majority carriers while crossing junction. Most of these carriers travel through the diode to reach the other end of the diode. This constitutes flow of current through the diode. Current on P side of diode is due to movement of holes and current on N side is due to movement of electrons. Both these currents constitute the current supplied by the battery.

This current will continue to flow as long as the battery is connected in the circuit.

If the battery voltage is increased, width of depletion region/potential barrier shall be further reduced. The majority carriers will gain more energy. A larger number of majority carriers will be able to cross over the barrier easily. Hence current flowing through the P-N junction diode will increase.

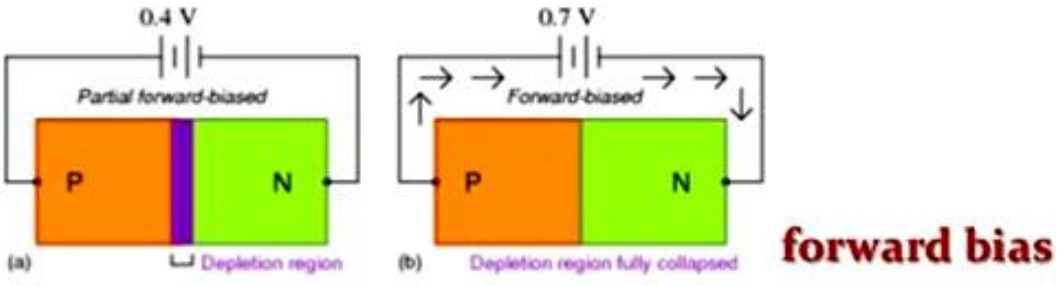


Fig.1.4:Forward biasing of diode

There is no resistance to movement of majority carriers in a forward biased diode. Thus a large number of majority carriers cross over the junction. This results to flow of a large current through the diode in Forward biased condition.

Reverse biased PN Diode

A diode is said to be reverse biased if its anode is connected to -ve terminal of battery and its cathode is connected to its +ve terminal of battery or electric supply.

or Reverse bias means when we try to make the current flow from n to p region of the diode. i.e. when p-side of diode is connected to -ve of battery and n-side of diode to +ve of the external battery. Here the barrier potential supports the external battery, So the depletion layer becomes wider. In this condition the current flow is due to minority carriers only.

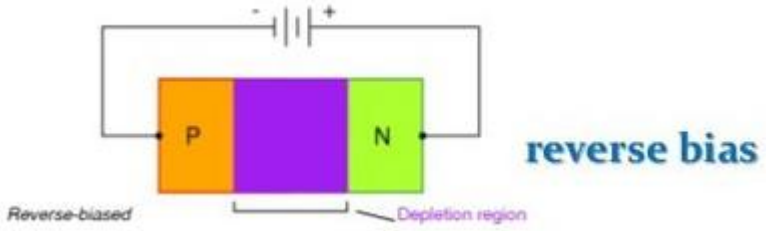


Fig1.5: Reverse bias of diode

Thus the diode offers very large resistance. The current remains low as the applied voltage is increased. This current is due to minority carriers and it is called reverse leakage current or reverse saturation current. When the applied voltage in reverse bias becomes too large the strong electric field causes breaking of the bonds. Thus the electron holes pairs in a large number are generated suddenly. It is known as the Zener breakdown. Reverse leakage current and Zener breakdown voltage both are very sensitive to temperature.

In addition to the Zener breakdown another kind of breakdown called the Avalanche breakdown is also observed in the p-n junction diodes. It takes place in lightly doped p-n junctions where the depletion layer is pretty wide. 1lhe electric field is quiet weak here and hence it cannot

produce a Zener breakdown. Rather the charge carries in the reverse biased condition gain kinematic energy from field and become strong enough to break a few bonds, In turn their number increases and in a short while yield multiplies. Thus an avalanche like situation is observed. That is why this quick rise in current is so caused.

1.2.7 DRIFT AND DIFFUSION CURRENT

When a voltage source, is connected to a semiconductor the electrons experience a force towards positive terminal and holes experiences an attraction towards negative terminal of the battery or source. In absence of the electric field the motion of electrons is in random direction but in presence of a source this random motion gets modified and a net movement of electrons and holes in opposite direction takes place. This motion is called a drift which makes a current called drift current. Though the electrons and holes move in opposite directions, but because of opposite charges on them the two currents called electron current and hole current are in same direction Thus the movement of charges under the influence of an electric field in a semiconductor is called drift current.

If in a semiconductor the carrier concentration is different from one region to another then a second type of current also exists. This current is also due to flow of electrons and holes which flows as a result of gradient of carrier concentration. This current is called diffusion current. This gradient of carrier concentration arises near the boundary of a P-N junction. Thus the movement of charges in a semiconductor device as a result of gradient of carrier concentration is called diffusion Current.)

1.2.8 V-I CHARACTERISTICS OF PN DIODE

The behavior of a diode under different conditions can be judged from it's V-I characteristics. It is a graph drawn between voltage applied to a diode and the current flowing through it.

Forward Characteristics

It is a graph drawn between voltage across terminals of a forward biased diode and current flowing through the diode at that time. Anode terminal (A) of diode is connected to +ve terminal of battery and cathode terminal (k) is connected to -ve terminal of battery, as shown in fig.1.6.

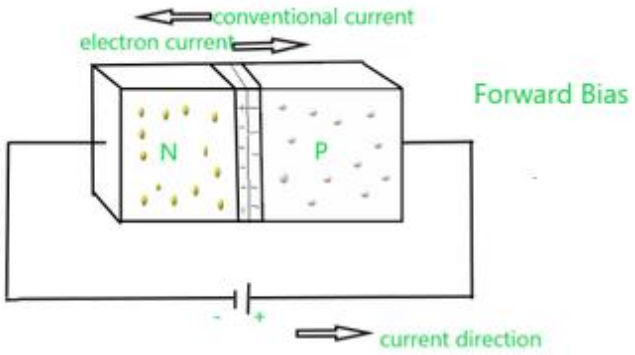


Fig.1.6 :Circuit to obtain forward characteristics of a diode

A potentiometer is connected across the battery to change the applied voltage. A resistance R is connected in the circuit to limit the current flowing through the forward biased diode. This resistance is essentially required in the circuit because a forward biased diode offers a very low

resistance. It will allow a very large current to flow if current limiting resistance is not provided. This high current if allowed to flow can damage the diode.

Voltage across the diode is measured by a voltmeter, t is an independent variable and is taken along the horizontal (x) axis. Forward current, the dependent variable is taken along y axis, Voltage applied to the diode is varied with the help of potentiometer provided in the circuit.

Different sets of voltage and current can be taken to draw the graph, Fig. shows the characteristics of a forward biased silicon diode. At low values of voltage across the diode, the current flowing through it is very small. This is due to potential barrier. As voltage across diode reaches 0.7 volts, larger number of majority carriers will be able to cross the junction thus increasing the current. Any further rise in voltage further increases the current flow.

Knee voltage: The voltage at which current through the diode increases rapidly is known as KNEE VOLTAGE or CUT IN voltage of diode. It is denoted by V_o and depends upon the semi conductor material used.

For Silicon Vo = 0.7 V Germanium Vo = 0.3 V

Maximum Forward Current: Current flowing through the diode produces heat. If very high current is allowed to flow through the diode, it may be damaged due to excessive heat. The maximum current that can safely flow through a forward biased diode is known as MAXIMUM FORWARD CURRENT. It is denoted by I_{FMAX}.

Reverse bias Characteristics

It is a graph drawn between voltage across terminals of a reverse biased diode and current flowing through the diode at that time. Anode terminal (A) of diode is connected to -ve terminal of Battery and cathode terminal (k) of diode is connected to +ve terminal of battery as shown in fig.1.7. A potentiometer is connected across the battery to change the applied voltage.

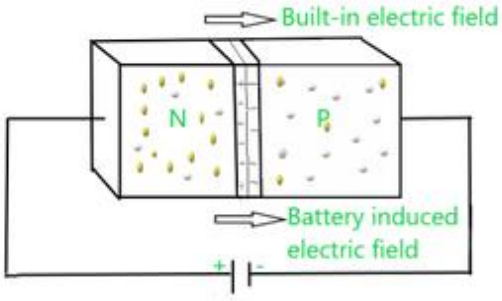


Fig.1.7 : Circuit to obtain Reverse characteristics of a diode

Voltage across the diode is taken along x-axis and current through it is taken along y-axis. A graph is drawn between these sets of values. Fig. shows the characteristics of a reverse biased diode. Current flowing through a reverse biased diode is very small. It flows due to movement of minority carriers across the junction. If the applied voltage increased. The current flowing does not change significantly. It is almost independent of voltage across the diode.

Break down voltage: If voltage across the reverse biased diode is further increased, breakdown occurs in the diode and current suddenly rises to a very high value. This voltage is

known as BREAKDOWN VOLTAGE. It is denoted by V_Z.Fig.1.8 shows complete characteristics of a diode.

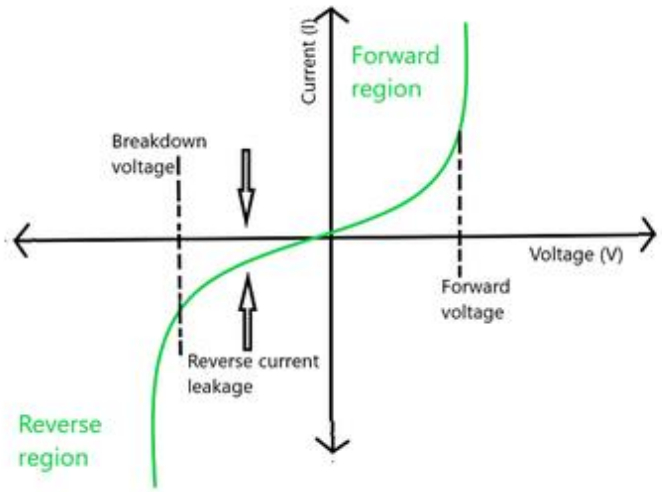


Fig.1.8 : V-I characteristics of a PN junction diode

From V-I characteristics of diode as shown in fig. it is concluded that current can flow through a diode in only one direction i.e. from anode to cathode. It conducts only in forward biased condition. This property of diode is known as UNIDIRECTIONAL property of diode. This property of diode is used in rectifier circuits discussed ahead.

1.3.1 Junction capacitance

Concept of junction capacitance in forward and reverse biased condition. The space charge region or depletion region of a reverse biased P-N junction has high resistivity. It is sandwiched between P region on one side and N region on the other side, having low resistivity. The P and N regions act as the plates of a capacitor, and the space-charge region acts as the dielectric. Thus, the P-N junction in reverse-bias has an effective capacitance, called transition or depletion capacitance.

1.3.2 ZENER DIODE

It is a heavily doped P-N junction designed to operate in reverse breakdown region. Reverse breakdown occurs in a zener diode at a fixed voltage known as zener breakdown voltage. The zener breakdown voltage can be controlled by controlling doping concentration of junction. Symbol of a Zener diode is shown in fig.1.9 below:-

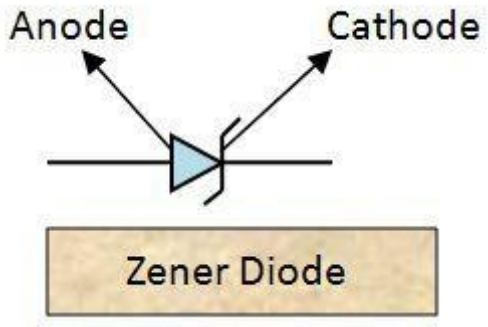


Fig.1.9: Symbol of a Zener diode

With a diode biased in the reverse direction, there can be two types of breakdowns

(a) Avalanche breakdown: This breakdown occurs in a lightly doped P-N junction. Such a Diode has a large depletion region. The minority carriers accelerated by the field of depletion region

collide with the semi-conductor atoms, breaking the covalent bonds and generating electron hole pairs. These new carriers acquire energy of the applied reverse voltage to produce additional carriers.It is a cumulative process, causing an avalanche breakdown.

(b) Zener breakdown: This breakdown occurs in a heavily doped P-N junction. Such a Diode has a thin depletion layer. A very strong electric field is set up at the depletion region on application of a reverse bias voltage. This field is strong enough to pull the electrons out of valances Orbit, generating a large number of electron hole pairs. This causes a high reverse current to flow .

The current increases sharply.

Zener breakdown is predominant at about 4 volts. Avalanche breakdown is predominant at about 6 volts. Between 4 to 6 volts, both breakdowns take place. The zener diode is not damaged due to the zener breakdown, Reverse characteristics of a zener diode are similar to that of a junction diodes. Zener diode is mostly used in voltage regulator circuit.

1.3.3 Characteristics of Zener diodes

The V-I Characteristics of a Zener Diode can be divided into two parts

(i) Forward Characteristics

(ii) Reverse Characteristics

Forward Characteristics

The forward characteristics of a Zener diode is shown in figure. It is almost identical to the forward characteristics of a P-N junction diode.

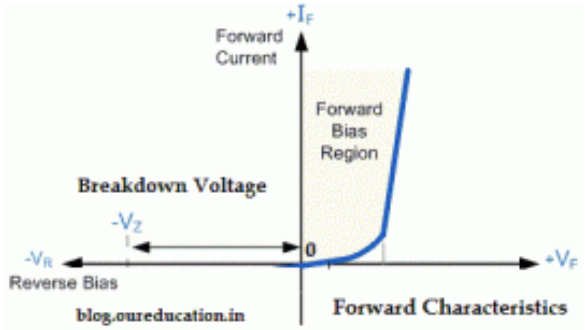


Fig.1.10:Forward Characteristics of Zener Diode

Reverse Characteristics

As we increase the reverse voltage, initially a small reverse saturation current Io. Which is in A, will follow. This current flows due to the thermally generated minority carriers. At a certain value of reverse voltage, the reverse current will increase suddenly and sharply . This is an indication that the breakdown has occurred. This breakdown voltage is called as Zener breakdown voltage or Zener voltage and it is denoted by V_z.

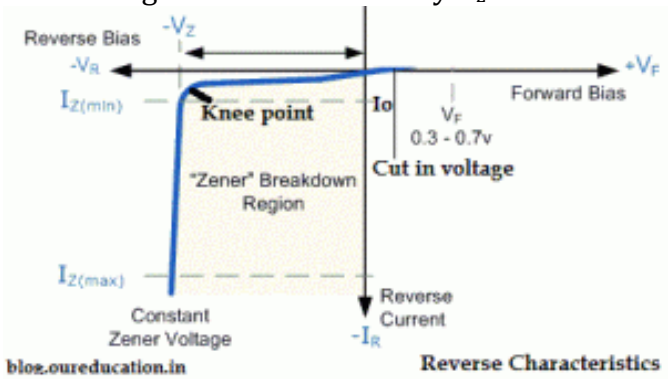


Fig.1.11:Reverse Characteristics of Zener Diode

The value of V_z can be precisely controlled by controlling the doping levels of P and N regions at the time of manufacturing a Zener diode. After breakdown has occurred. The voltage across Zener diode remains constant equal to V_z. Any increase in the source voltage will result in the increase in reverse Zener current. The Zener current after the reverse breakdown must be controlled by connecting a resistor R as shown in figure. This is essential to avoid any damage to the device due to excessive heating.

Zener Region and its importance

Reverse breakdown of the zener diode operates in a region called zener region, as shown in figure. In this region the voltage across zener diode remains constant but current changes depending on the supply voltage. zener diode is operated in this region when it is being used as a voltage regulator. The complete v-i characteristics of zener diode is as shown in figure 1.12.

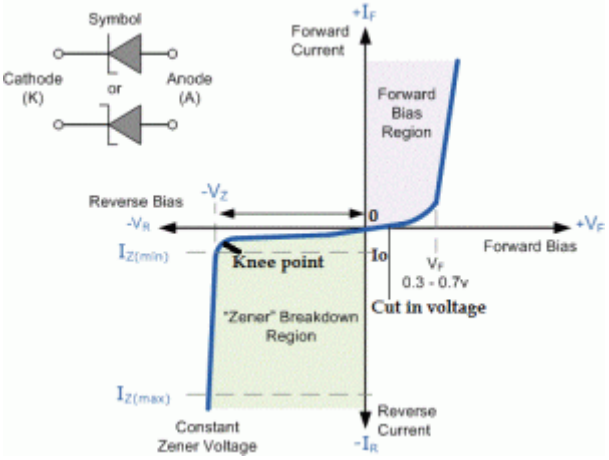


Fig.1.12:V-I Characteristics of Zener Diode

1.3.4 Applications of Zener diode:

1. It is normally used as voltage regulator.
2. Used as voltage reference.
3. Used in switching operations.
4. Used in clipping and clamping circuits.
5. Used in protective circuits.

1.4 Diode as rectifier:- A rectifier converts alternating voltage into direct voltage. A p-n junction diode is a useful type of rectifier as it would not conduct in both halves i.e. positive as well as negative halves of input voltage when connected to a source of a.c.

There are three basic types of rectifiers,

(i) Half wave rectifier: It uses only one diode. It merely chops the -ve half cycle of a.c., thus the output current is a unidirectional but discontinuous current.

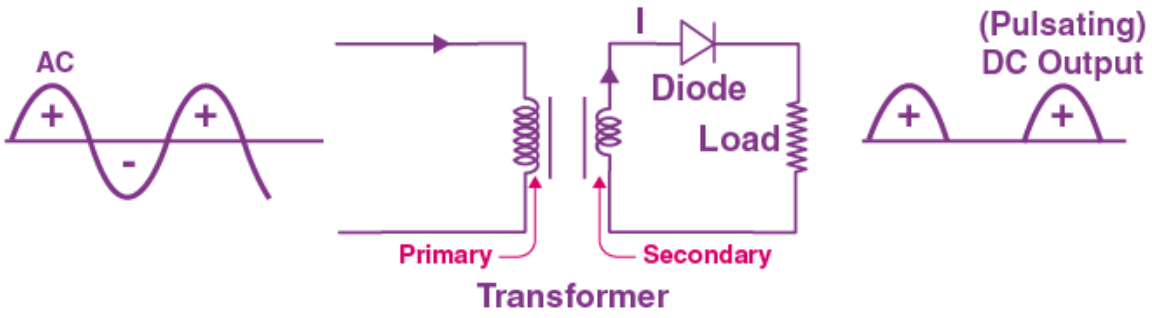


Fig.1.13:Half Wave Rectifier

In addition the output periodically increases and decreases. It has a high ripple factor of 1.21 and low efficiency~40%.

(ii) Full wave rectifier: It uses two identical p-n junction diodes. These diodes alternately conduct for positive and negative half cycles of the input a.c. Thus the output is continuous but pulsating d.c.

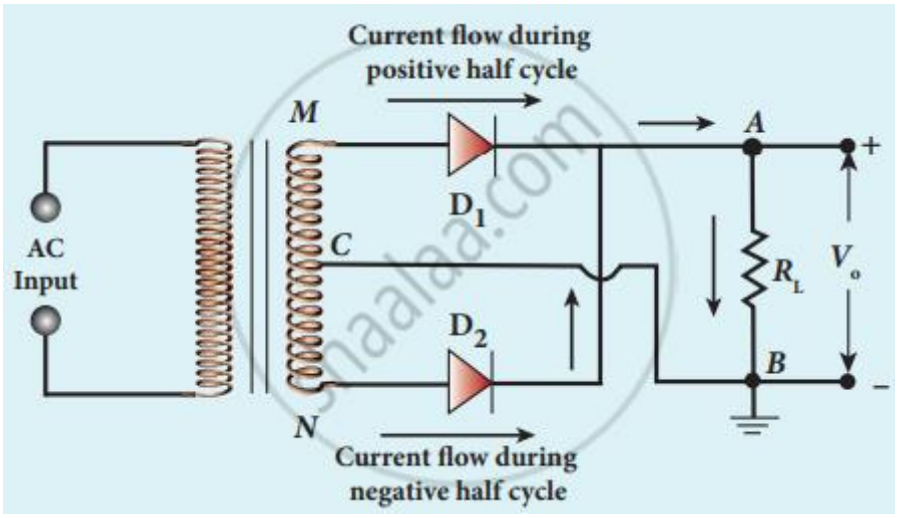


Fig.1.14:Center tapped Full Wave Rectifier

It has a much lower ripple factor of 0.482 and better efficiency, 81.2%. A major problem with his kind of rectifier is that one requires transformer of double voltage rating as compared to the output e.g, to get an output of 6 volt d.c. a power supply having full wave rectifier needs to have a transformer secondary rating 6-0-6 volt i.e. 12 volt in total.

(iii) Bridge rectifier : This kind of rectifier gives full wave rectification with a continuous but pulsating d.c. but it uses four diodes.

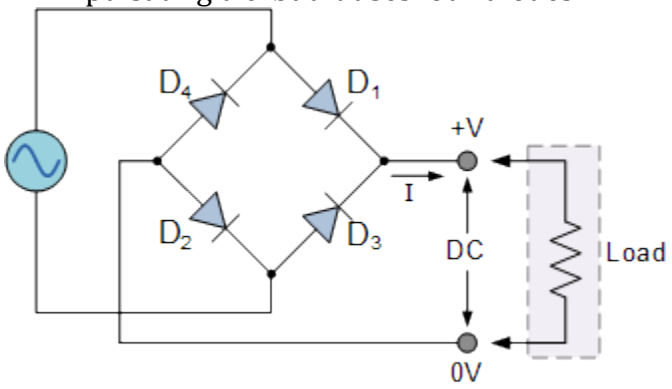


Fig.1.15:Full Wave Bridge Rectifier

The advantage is that the transformer required is of same secondary voltage rating as that of the output. i.e. for a 6 volt d.c. transformer secondary needed is of 6 volt only. The ripple factor and PIV same as those in the case of a two diode full wave rectifier.

1.4.1 Ripple factor calculations

RIPPLE:- The time varying component of output is called RIPPLE.

Ripple factor: It is the ratio of a.c. component or time varying component of current to the d.c. current of a wave. For a half wave rectifier:- R=1.21

It is observed that ripple voltage or current is more than d.c. voltage or current in a half wave rectifier. Hence it is not a good rectifier. For Full wave rectifier the RIPPLE factor is 0.482.Compared with the value of ripple factor of a half wave rectifier (whose value is 1.21). The ripples or time varying component of current has largely reduced.

1.4.2 Efficiency of rectification: lt is the ratio of output d.c. power of the circuit to its input a.c. power. Efficiency of rectification = 40.6% for half wave rectifier. This is the max. efficiency at which a half wave rectifier can work. Power loss in transformer secondary winding and diode has been neglected. Only 40.6% of input power is converted in d.c .power in a half wave rectifier. Rectification Efficiency : For a full wave rectifier =81.2 %. Rectification efficiency of a full wave rectifier is twice that of a half wave rectifier under identical conditions. The maximum possible efficiency can be 81.2% (when $r_a << R$).

1.4.3 Peak inverse voltage: It is the maximum voltage which appears across the diode when it is not conducting. In a half wave rectifier, maximum voltage which appears across the diode during non-conducting stage is V_m.

PIV of diode = V_m

Peak inverse voltage is a very important specification of diode. It helps in deciding, the maximum voltage for which a diode can be used.

Peak Inverse Voltage For Full wave rectifier. As shown in fig. diode D_1 is in non-conduction stage. At the instant when secondary voltage reaches it's maximum value, whole of V_m appears across R_L due to conduction of D_2.

Hence voltage across non conducting diode D_1 is sum of voltage across half of secondary Winding and voltage across R_L.

PIV $=V_m-(-V_m)$

$=V_m + V_m=2\ V_m$

When compared with PIV of a half wave rectifier, it is twice the PIV rating in a half wave rectifier circuit.

1.4.4 FILTER CIRCUITS

Rectifiers are used to convert a.c. into d.c. The output of rectifier circuits is not purely d.c. it is pulsating d.c. It contains a.c. component or ripple component. The ripple component is higher for a half wave rectifier compared to full wave rectifier.

Most of the electronic circuits require smooth d.c. for their operation. Hence the ripple components must be reduced to make the output of rectifier useful in these circuits.

Following filter circuits are used for filtration of a.c. component of output of rectifier:

(i) Inductor filter
(ii) Shunt capacitor filter
(iii) Inductor capacitor filter or L-C filter
(iv) π filter
(v) T filter

Inductor Filter

An inductor has the property to oppose any change of current flowing through it. Whenever current flowing through an inductor changes, an e.m.f. is induced. The induced e.m.f. opposes the change in current as per Lenz's Law. This property is used in inductor filter circuits to reduce the variations in rectified current, thus reducing the ripples.

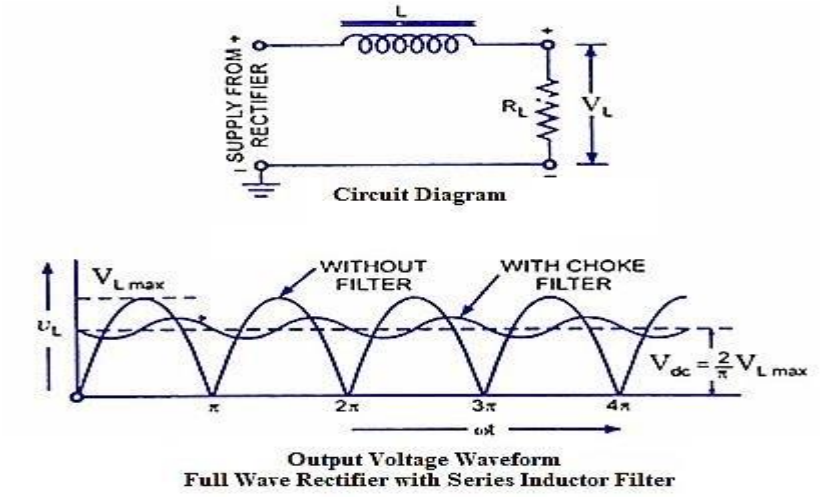


Fig.1.16: Inductor Filter

Inductor offers a very low resistance to d.c. while impedance offered to a.c. is high depending upon frequency of supply.

Shunt Capacitor Filter

The capacitive reactance of a capacitor =1\2πfc .At low frequencies a capacitor offers a high reactance, while at high frequencies a capacitor offers a low reactance. A capacitor offers almost open circuit (High reactance) to d.c. and almost short circuit (Low reactance) to a.c.

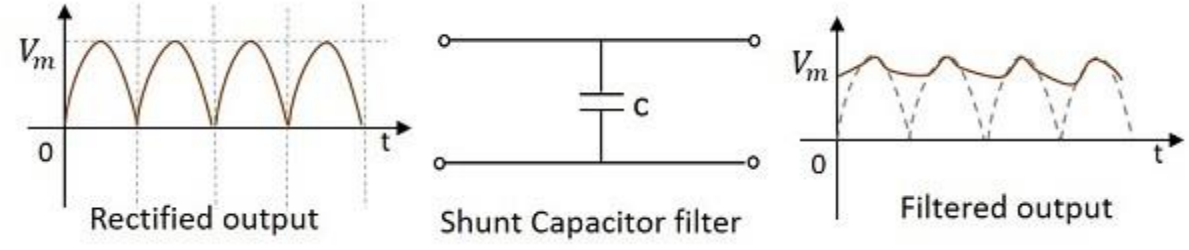


Fig.1.17: Shunt Capacitor Filter

Thus it allows flow of a.c. through it while restricts the flow of d.c. Only a small component of a.c. passes through load, thus reducing the ripple component. This property of capacitor is used in shunt capacitor filters. A high value capacitance C is connected across the load resistance.

EXERCISE UNIT – 1

OBJECTIVE TYPE QUESTION

SECTION –A

Objective Type Questions

Fill in the blanks

1. The electrons in the outermost orbit are called….. electrons.
2. The merging of a free electron and a hole is called…..
3. Free electrons are the…..carriers in N type semiconductors, and holes are the….. carriers.

4. Semiconductors have….bonds.
5. A semiconductor has….temperature coefficient of resistance.
6. With the addition of pentavalent impurity to semiconductor, ….. semiconductor is obtained.
7. In N-type semiconductor, ……..are the minority carriers.
8. The majority carriers in P-type semiconductor are…….
9. The value of knee voltage for silicon diode is…. Volt.
10. A crystal diode acts as an ……. Switch.
11.A bridge rectifier circuit is not suitable for….. voltage rectification. (low/high)
12. The maximum efficiency of full wave rectifier is…..
13. A capacitor circuit does not allow to pass….. component. (a.c./d.c.)
14. Zener diode is made to operate in …….. region.
15. Usually, a zener diode is used as a ….
16. …. Diode has a -ve resistance.
17.Filter circuits are used to reduce…….
18.The reverse saturation current occurs due to movement of….
19. Zener diodes are used as….
20. The ripple factor in a full wave rectifier is….
21. In a p-type semi-conductor…..are majority carriers.

ANSWERS

Fill in the blanks

1. Valence	2. Recombination	3. Majority, Minority	4. Covalent
5. Negative	6. N-type	7. Electron	8. Holes
9. 07	10. Electronic	11. Low	12. 81.2%
13. d.c.	14. Breakdown	15. Voltage regulator	16. Tunnel
17. Ripples/ac. Components		18. Minority carriers	19. Voltage regulators
20. 0.482	21. Holes		

Multiple Choice Questions:

Q. 1 The PN junction behaves like a
a) resistor b) diode
c) triode d) tetrode.

Q. 2 When a high reverse voltage is applied to a PN Junction
a) it becomes a transistor b) avalanche breakdown occurs
c) zener breakdown occurs d) None of these.

Q. 3 The reverse saturation current in a PN-junction under reverse bias
a) increases b) decreases
c) remains constant d) None of these.

Q. 4 In the depletion region of PN-junction, there are
a) no mobile charges b) no charges
c) no currents d) All of these.

Q. 5 A Zener diode is used as

a) an amplifier b) a voltage regulator

c) a coupler d) a rectifier

Q. 6 An intrinsic semiconductor at absolute zero temperature

(a) behaves like an insulator

(b) has a large number of holes.

(c) has a few holes and same number of electrons.

(d) Behaves like a metallic conductor.

Q. 7 There is no hole current in good conductors because they

(a)Have overlapping of valence and conduction bands.

(b)Are full of electron gas

(c)have large forbidden energy gap

(d)Have no valence band.

Q. 8 In P-type semiconductor, there

(a)No majority carriers (b)Electrons as majority carriers.

(c) immobile negative ions (d)immobile positive ions

Q. 9 In N-type semiconductor, there are

(a)No majority carriers (b)Holes as majority carriers

(c) immobile negative ions (d)Immobile positive ions

Q. 10 Donor type semiconductor is formed by adding impurity of valency

(a)3 (b)4

(c)5 (d)6

Q. 11 Acceptor type semiconductor is formed by adding impurity of valances

(a) 3 (b) 4

(c)5 (d)6

Q. 12 In a crystal diode, the barrier potential offers opposition to only

(a)Free electrons in n-region (b) Holes in p-region

(c) majority carriers in both regions (d) minority carriers in both regions.

Q. 13 When a reverse bias is applied to a crystal diode, it

(a) raises the potential barrier

(b) lowers the potential barrier

(c) increases the majority-carrier current greatly

(d) None of these.

Q. 14 At reverse bias, the number of minority carriers crossing the junction of a diode depends primarily on the

(a) Concentration of doping impurities

(b) rate of thermal generation of electron-hole pairs.

(c) magnitude of the potential barrier

(d) all of these.

Q. 15 When a pn junction is forward biased

(a) electrons in the n-region are injected into the p-region.

(b) holes in the p-region are injected into the n-region.

(c) both a and b

(d)None of these.

SHORT TYPE QUESTION

SECTION – B

Q. 1 Name two commonly used semiconductors.
Q. 2 Write a short note on PN Junction Diode?
Q. 3 Discuss methods of biasing of diode. Explain forward bias and reverse bias ?
Q. 4 Describe rectifier in details.
Q. 5 Define filter. Explain inductor and shunt capacitor filter?
Q.6 Differentiate between drift and diffusion current?
Q.7Differentiate between zener breakdown and avalanche breakdown?
Q.8 Define zener diode. Explain V-I characteristics of zener diode.
Q.9 Explain current mechanism of PN junction diode.
Q.10.Define semiconductor. Explain different type of semiconductor.
Q. 11 What is charge carriers? Explain minority and majority charge carrier.
Q.12 write a short note on Junction capacitance, Potential barrier, depletion layer and doping.

LONG TYPE QUESTION

SECTION – C

Q. 1 Explain the difference insulators and semi-conductors using the energy-band diagrams?
Q. 2 Discuss diode as rectifier. Describe diode as half-wave, full wave and bridge rectifiers. Write a short note on Peak Inverse Voltage, rectification efficiencies and ripple factor also.

Answer of section A

1. (b)	2. (c)	3. (c)	4. (a)	5. (b)	6. (a)
7. (a)	8. (c)	9. (d)	10. (c)	11. (a)	12. (c)
13. (a)	14. (b)	15. (c)			

UNIT II: Introduction to Bipolar Transistors

2.1 Concept of a bipolar transistor

A bipolar junction transistor is formed by introducing opposite type of impurities through two opposite faces of a predoped slice of a semiconductor. E.g. if a p-doped slice is taken and N-type impurities are introduced into its two faces, some of the region on each face will become n-type. Thus n-p-n transistor will be formed. Similarly by starting with n-type slice a p-n-p transistor can be formed.

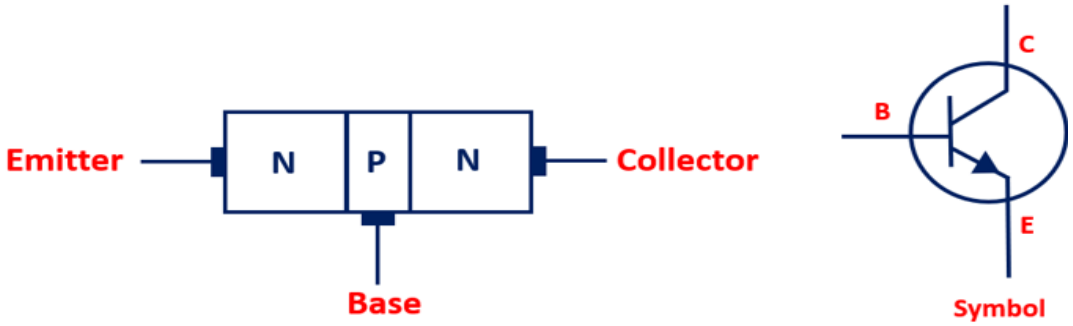


Fig.2.1:NPN transistor and their symbol

A transistor is a three terminal device, with two p-n junctions formed back to back. The three terminals are leads to three regions of the transistor namely emitter, base and collector.

The emitter as the name suggests, is used to inject the charge carriers into the transistor, mostly it is on the input side. The collector is used to collect the charge carriers for output stage. The base serves as a control for the flow of charge carriers. The base is lightly doped as compared to rich doping of emitter and collector. The base is also made very thin. The collector is mostly the largest region, as it is supposed to handle a large power (relatively).

Two p-n junction diodes connected back to back can not make a transistor to be thin and lightly doped. The transistor needs two power sources for biasing. The biasing rule is "emitter is forward biased and collector is reverse biased.

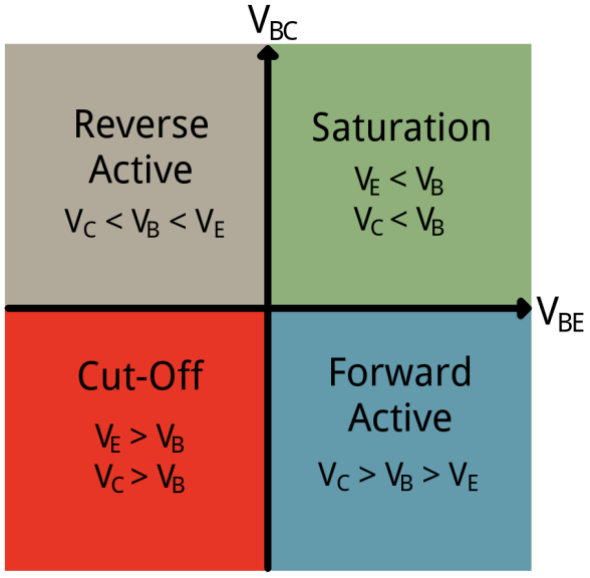


Fig.2.2:Different Regions in BJT

When emitter of a transistor is kept in open circuit and collector is reverse biased the leakage current is called collector leakage current, I_{CBO} During any operation, as its large value can burn the transistor.

A transistor obeys Kirchhoff's current law when it is wired in a circuit, i.e. the equation $I_E=I_B+I_c$ is valid.

Transistor is basically an amplifier. Its name has been derived from the term 'Transfer Resistor'. The low resistance in its input side and high resistance in its output side makes it an ideal amplifier of current, voltage and power.

Structure of BJT

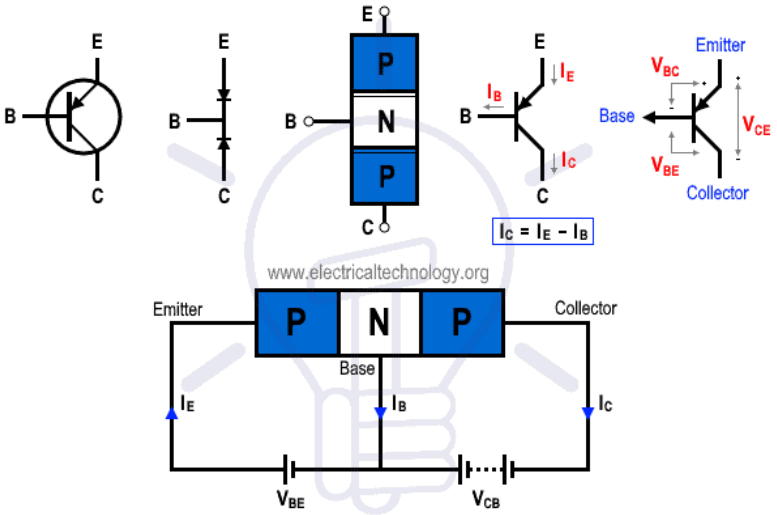


Fig.2.3:Construction & Working of PNP transistor

PNP and NPN transistors,
Transistors Symbols
Concept of leakage current

2.2 Configurations of a transistor

CB, CE, CC configurations of a transistor:
Transistor can be connected in three basic configurations, common base, common emitter and common collector. The last one is rarely used.
In common base configuration we have common base current gain =0.95 or less the transistor would act as voltage amplifier.
In common emitter configuration, the current gain is denoted by, Beta=$\Delta I_C/\Delta I_B$
The current gains alpha and Beta are related to each other as, Beta=Ratio of Alpha and (1- Alpha)
Input resistance in CB is comparatively smaller than that in CE configuration
Output resistance in CB configuration is very high. But in CE configuration, output resistance is not very high (8 k Q). It also depends on choice of the operating point.
Value of CB current gain, a is 0.98 but in case of CE configuration B ranges from 50 to 250.

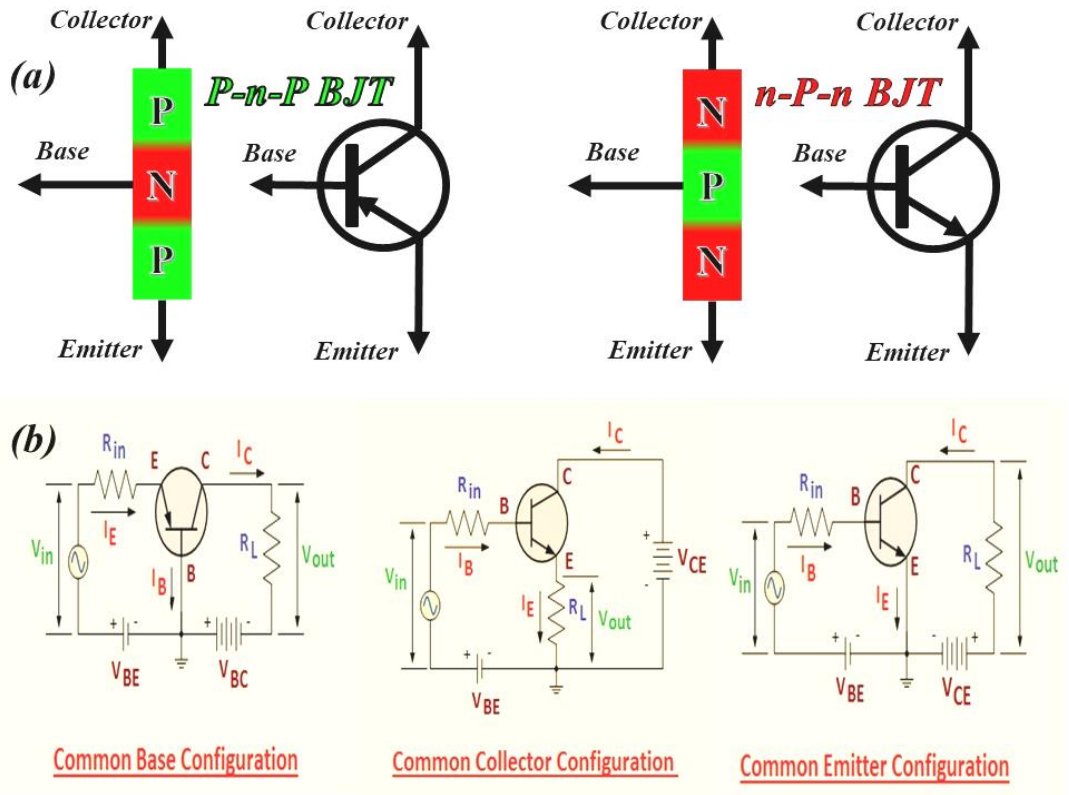


Fig.2.4:Configuration of BJT

In CB configuration, the leakage current is very low while in CE configuration it is relatively higher. The leakage current is function of temperature as well.

CB base amplifier has very low input resistance and very high output resistance but it is not so in case of CE amplifier i.e. input resistances is low while output resistance is high.

In CB amplifier, there is no phase shift between input and output. But in CE amplifier, there is a phase shift of 180°

Input and output characteristics in CB configurations

Input characteristics of transistor in CB and CE configuration both, show the forward biased emitter. In a way they are like the characteristics of a forward biased p-n junction.

Output characteristics in CB and CE configuration are like reverse biased collector. They look like those of a reverse biased p-n junction (looking upside down). These characteristics have three principal regions saturation, cut off and active. A transistor has to be biased in the active region so as to act as an amplifier.

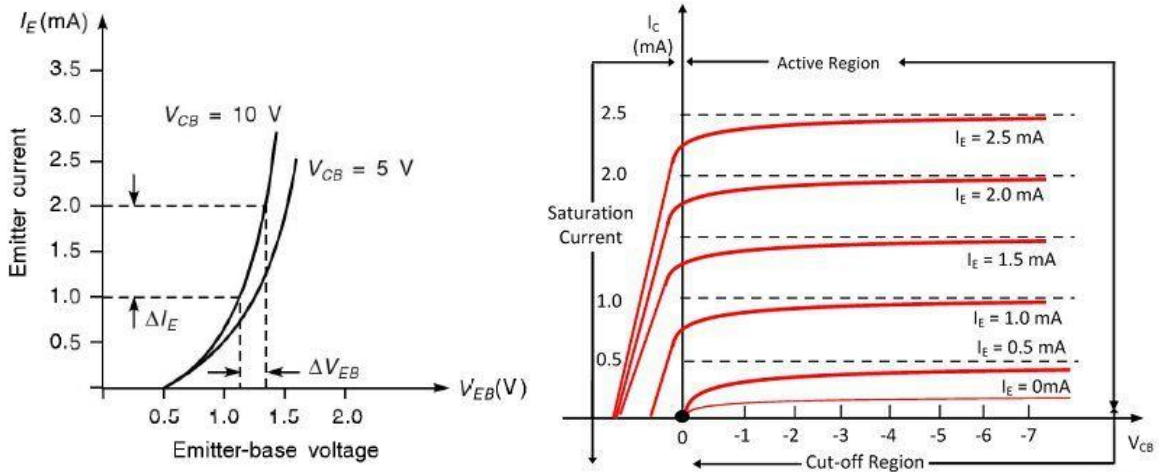


Fig.2.5: Input and output characteristics in CB configurations

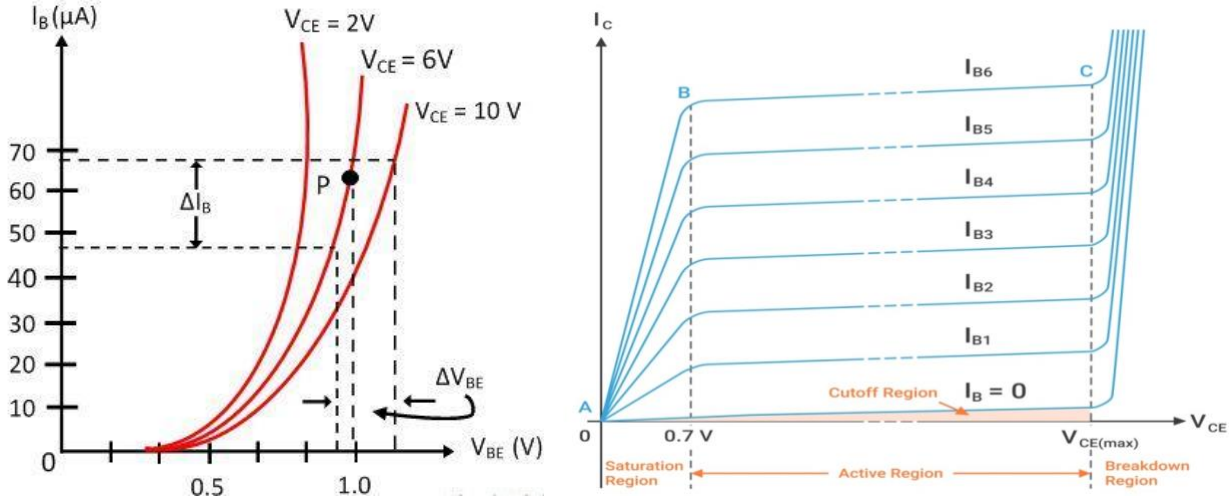


Fig.2.6:Input and output characteristics in CE configurations

2.3 Transistor as an amplifier in CE Configuration

During the positive half-cycle of the signal, the forward bias across the emitter-base junction is increased. Therefore, more electrons flow from the emitter to the collector via the base. This causes an increase in collector current.

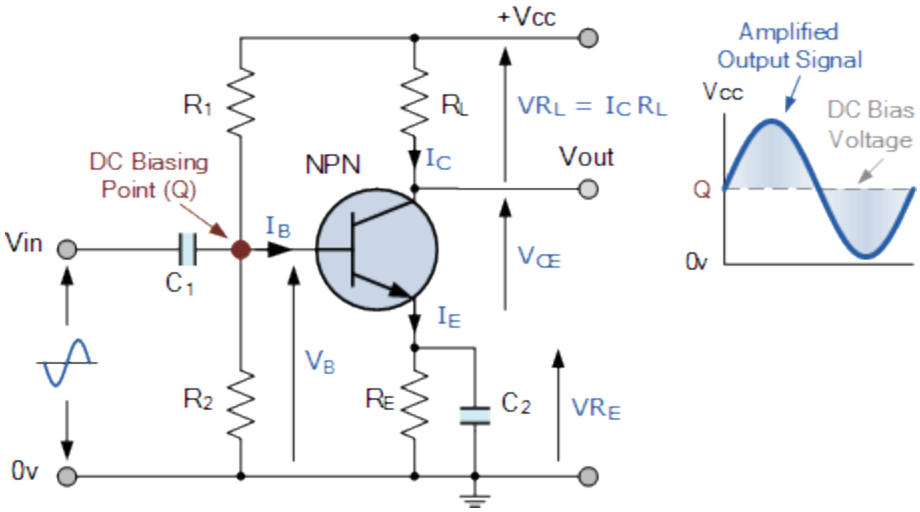


Fig2.7: Transistor as an amplifier Circuit

The increased collector current produces a greater voltage drop across the collector load resistance RC. However, during the negative half-cycle of the signal, the forward bias across emitter-base junction is decreased. Therefore, collector current decreases. This results in the decreased output voltage (in the opposite direction). Hence, an amplified output is obtained across the load.

Current amplification factors
Relation b/w α, β and γ

(a) Between α and β

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

$$I_E = I_C + I_B$$
$$\Delta I_E = \Delta I_C + \Delta I_B$$
$$\Delta I_B = \Delta I_E - \Delta I_C$$

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C}$$

Divide numerator and denominator by ΔI_E

$$\beta = \frac{\frac{\Delta I_C}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{\alpha}{1-\alpha}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

(b) Between β and γ

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

$$I_E = I_C + I_B$$
$$\Delta I_E = \Delta I_C + \Delta I_B$$
$$\gamma = \frac{\Delta I_C + \Delta I_B}{\Delta I_B}$$

$$= \frac{\Delta I_C}{\Delta I_B} + 1 = \beta + 1$$
$$\gamma = \beta + 1$$

(c) Relation between α, β and γ

$$\beta = \frac{\alpha}{1-\alpha}$$

Add 1 to both sides

$$\beta + 1 = \frac{\alpha}{1-\alpha} + 1 = \frac{1}{1-\alpha}$$

$$\gamma = \beta + 1 = \frac{1}{1-\alpha}$$

Comparison of CB, CE and CC Configurations

Characteristics	Common base	Common emitter	Common collector
Input resistance	Low (100Ω)	Low (750Ω)	Very high (≅ 750 KΩ)
Output resistance	Very high (≅ 400 KΩ)	High (≅ 50 KΩ)	Low (≅ 50 Ω)
Voltage gain	≅ 150	≅ 500	Less than 1
Output phase	Same phase	Opposite Phase	
Current Amplification	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
Factor or current gain	$\alpha < 1$	$\beta > 1$	$\gamma > 1$
Voltage gain	$A_V = \frac{V_O}{V_i} = \frac{I_C R_L}{I_E R_i}$ $A_V = \alpha \frac{R_L}{R_i}$	$A_V = \frac{V_O}{V_i} = \frac{I_C R_L}{I_B R_i}$ $A_V = \beta \frac{R_L}{R_i}$	Not used for amplification
Power gain	$A_P = \frac{P_O}{P_i}$ $A_P = \alpha^2 \frac{R_L}{R_i}$	$A_P = \frac{P_O}{P_i}$ $A_P = \beta^2 \frac{R_L}{R_i}$	Not used for amplification
Application	For high frequency	For audio frequency	For Impedance

EXERCISE UNIT – 2
OBJECTIVE TYPE QUESTION

SECTION –A

Objective Type Questions

Fill in the blanks

1. A transistor contains.... PN-junctions.
2 In a transistor, base is made very.... and it is ..... doped.
3. The most commonly used transistor circuit is.....
4 In any transistor circuit, Ig = ... + ...
5. In a transistor, the value of alpha is always.....than one.
6.The formula for current gain(alpha) = .
7. In the saturation region of a transistor, both the junctions are .....
8. The value of collector current of a transistor is..... to emitter current. (less/more/equal)

ANSWERS

Fill in the blanks :

1. two 2. thin, lightly 3. common emitter 4. Ic + IB 5. Less 6. {B/(1+B)}i.e B means beta
7. forward biased 8. nearly equal.

Multiple Choice Questions:

Q.1 In common emitter configuration power gain is
(a) less than unity (b) low
(c) medium (d) high

Q.2 In common collector configuration current gain is
(a) very low (between 0.9 to 1.0)
(b) low (about 5)
(c) high (near by 20)
(d) very high (near by 80)

Q.3 CE configuration is preferred when main criterion is
(a) voltage gain
(b) both voltage gan and current gain
(c) output impedance
(d) input impedance

Q.4 The most commonly used transistor circuit arrangement is
(a) common emitter
(b) common base
(c) common collector
(d) all of the above three equally

Q.5 The collector characteristics of a common emitter connected transistor may be used for determination of
(a) input resistance
(b) output resistance
(c) base current
(d) voltage gain

Q.6 A transistor is said to be in a quiescent state when
(a) no signal is applied to the input
(b) it is unbiased
(c) no currents are flowing
(d) emitter junction bias is just equal to collector junction bias

Q.7 When a positive voltage signal is applied to the base of a normally biased NPN common-emitter transistor amplifier
(a) the emitter current decreases
(b) the collector voltage becomes less positive
(c) the base current decreases
(d) the collector current decreases

Q.8 In transistor, alpha is

(a) small signal voltage gain of a CE transistor
(b) large signal current gain of a CE transistor
(c) large signal voltage gain of a CE transistor
(d) small signal current gain of a CB transistor

Q.9 In a bipolar transistor the configuration that have both current and voltage gain high,
(a) CB (b) CC
(c) CE (d) both (b) and (c)

Q.10 The circuit arrangement of a transistor used as a buffer is
(a) CE (b) CB
(c) CC (d) any of the above three

Q.11 The input and output signals of a CE transistor amplifier are
(a) always equal (b) always -ve
(c) always in phase (d) out of phase

Q.12 A transistor is a combination of two PN-junction with their
(a) P-regions connected together
(b) N-regions connected together
(c) N-regions connected to P-regions of other
(d) Both (a) and (b).

Q.13 The arrow in a transistor symbol indicates the direction of current in
(a) emitter (b) base
(c) collector (d) none of these.

Q.14 The transistors are:
(a) low voltage and high current devices
(b) low voltage and low current devices
(c) high voltage and high current devices
(d) only high current devices.

Q.15 The batteries are connected to a transistor in such a way that the two PN-Junction of the transistor
(a) are forward biased
(b) are reversed biased
(c) one junction is forward biased while the other is reverse biased
(d) none of these.

Q.16 In a transistor:
(a) the conductivity of emitter is higher than that of base
(b) the conductivity of emitter is lower.than that of base

(c) the conductivity of both emitter and base is same
(d)None of these

SHORT TYPE QUESTION

SECTION – B

Q.1 Draw a sketch showing the structure of an NPN junction transistor. Label the emitter, base and collector regions. Also label the emitter-base and collector base junctions.
Q.2 Show the biasing arrangement for a PNP transistor in CB configuration so that it works in active region.
Q.3 Explain the function of the emitter, base and collector in the operation of a junction transistor
Q.4 Though the collector-base junction of a transistor operating in active region is reverse-biased, the collector current is still quite large. Give reason.
Q.5 What causes collector current to flow when the emitter current is zero? What is this collector current called? How does temperature affect it?
Q.6 Draw an NPN transistor in the CB configuration biased for operation in active region.
Q.7 Sketch typical CB input characteristic curves for an NPN transistor. Label all variables. How you will calculate the input dynamic resistance of the transistor from these curves?
Q.8 Draw circuit of NPN Transistor in CE configuration. Show polarity of batteries and all other voltages. Mark direction of various currents in the circuit.
Q.9 Sketch typical CE input characteristics for an NPN transistor. How will you calculate the input dynamic resistance of the transistor at a given point from these curves?
Q.10 Derive the relationship between the beta, alpha and gamma of a transistor.
Q.11 Explain why CE configuration is most popular in amplifier circuits.
Q.12 Draw the circuit diagram of a transistor amplifier in CE configuration.

LONG TYPE QUESTION

SECTION – C

Q. 1 Describe how you will determine the voltage gain of the CE amplifier by plotting the DC load line on the output characteristics of the transistor?

Q. 2 Sketch typical CE output characteristic curves for an NPN transistor. How you will compare the value of beta of the transistor from these characteristic curves?

Answer of section A

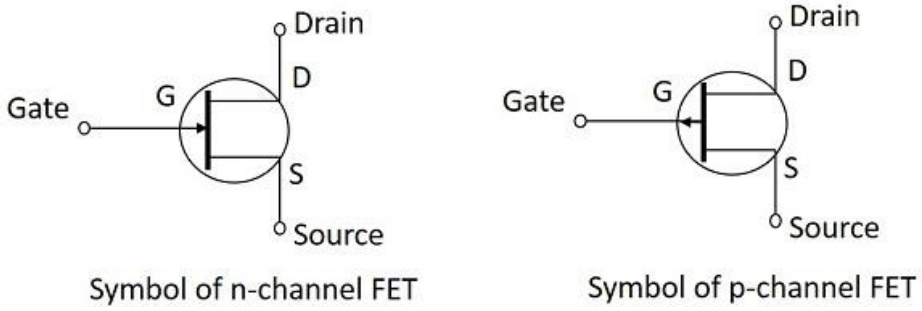
1. (d)	2. (d)	3. (b)	4. (a)	5. (b)	6. (a)
7. (b)	8. (d)	9. (c)	10. (c)	11. (d)	12. (d)
13. (a)	14. (b)	15. (c)	16. (a)		

UNIT III: Field Effect Transistors

3.1 FIELD EFFECT TRANSISTOR

INTRODUCTION

Field effect transistor has a channel of P-type semiconductor or N-type semiconductor. Two heavily doped regions of opposite polarity semiconductor material (N-type for P channel and P-type for N channel) are formed on either sides of channel. A common terminal is taken out from it, known as gate. Two leads taken from two ends of channel form source and drain terminals. Thus a field effect transistor abbreviated as FET is a three terminal device.



Symbol of n-channel FET Symbol of p-channel FET

Fig.3.1:Symbols of FET

Gate terminal of FET is similar to base terminal, source terminal is similar to emitter terminal while drain terminal is similar to collector terminal of junction transistor. It is a unipolar device. Its operation depends on flow of majority carriers through the channel.

A junction transistor is a current controlled device. It's operation is controlled by base current. FET is a voltage controlled device. It's output characteristics are controlled by input voltage. **FETs can be classified as**

1. JFET(N-channel & P-channel)
2. MOSFET(IGFET)
   (i) Depletion type(N-channel & P-channel)
   (ii) Enhancement type(N-channel & P-channel)

(IGFET- Insulated Gate Field Effect Transistor)

MOSFET- Metal Oxide Semiconductor Field Effect Transistor)

Advantages of FET over a junction transistor :

1. High input impedance: FET has high input impedance of the order of 100 Mega ohms for a JFET to 10^{15} ohms for a MOSFET.
2. FET is a voltage controlled device.
3. Noise level in FET is lower than that of junction transistor.
4. It has better thermal stability.
5. Fabrication of FET is simpler.
6. It occupies lesser space.

Disadvantages of FET over junction transistor.

1. Gain of FET amplifier is lower than a transistor amplifier.
2. Cost of FET is higher than transistor.
3. Gain Band width product of FET is lower than transistor.

Construction of FETs

The N-channel FET is the mostly used Field Effect Transistor. For the fabrication of N channel FET, a narrow bar of N-type semiconductor is taken on which P-type material is formed by diffusion on the opposite sides. These two sides are joined to draw a single connection for gate terminal. This can be understood from the following figure.

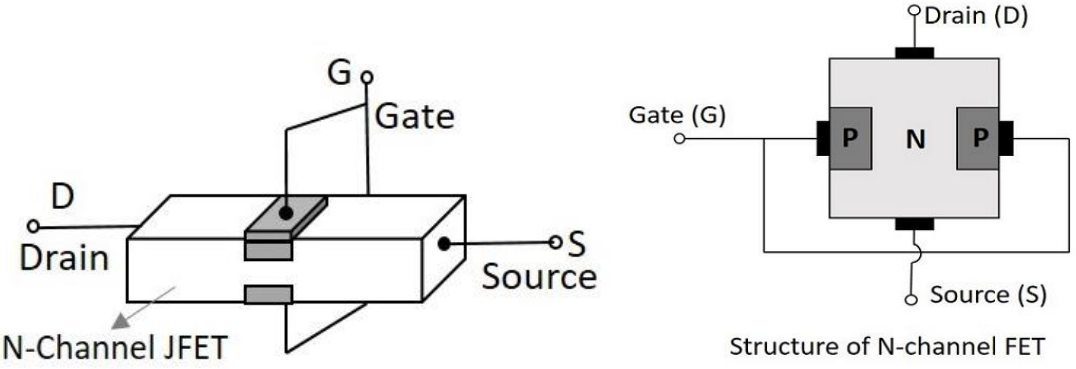


Fig.3.2: Construction of FETs

These two gate depositions p–type materials form two PN diodes. The area between gates is called as a channel. The majority carriers pass through this channel. Ohmic contacts are made at the two ends of the n-type semiconductor bar, which form the source and the drain. The source and the drain terminals may be interchanged.

Operation of FETs

When both the supplies are given. The supply at gate terminal makes the depletion layer grow and the voltage at drain terminal allows the drain current from source to drain terminal. Suppose the point at source terminal is B and the point at drain terminal is A, then the resistance of the channel will be such that the voltage drop at the terminal A is greater than the voltage drop at the terminal B. Which means $V_A > V_B$

Hence the voltage drop is being progressive through the length of the channel. So, the reverse biasing effect is stronger at drain terminal than at the source terminal. This is why the depletion layer tends to penetrate more into the channel at point A than at point B, when both V_{GG} and V_{DD} are applied. The following figure3.3 explains this.

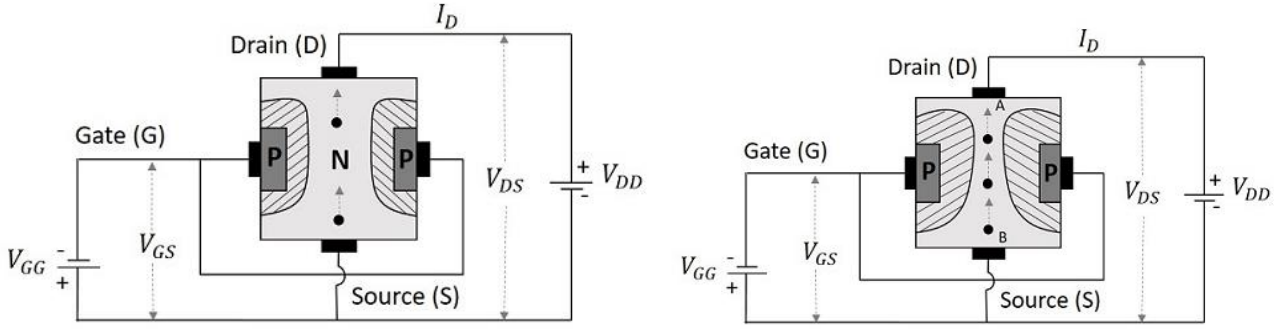


Fig.3.3: Operational View Of JFET

When this drain current is further increased, a stage occurs where both the depletion layers touch each other, and prevent the current I_D flow. This is clearly shown in the following fig.3.4.

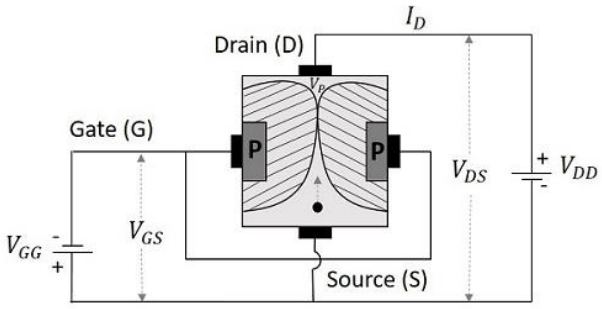


Fig.3.4:When V_{GG} and V_{DD} are very high

The voltage at which both these depletion layers literally "touch" is called as "Pinch off voltage". It is indicated as V_P. The drain current is literally nil at this point. Hence the drain current is a function of reverse bias voltage at gate

Characteristics of FETs

When the voltage between gate and source V_{GS} is zero, or they are shorted, the current I_D from source to drain is also nil as there is no V_{DS} applied. As the voltage between drain and source V_{DS} is increased, the current flow I_D from source to drain increases. This increase in current is linear up to a certain point A, known as Knee Voltage.

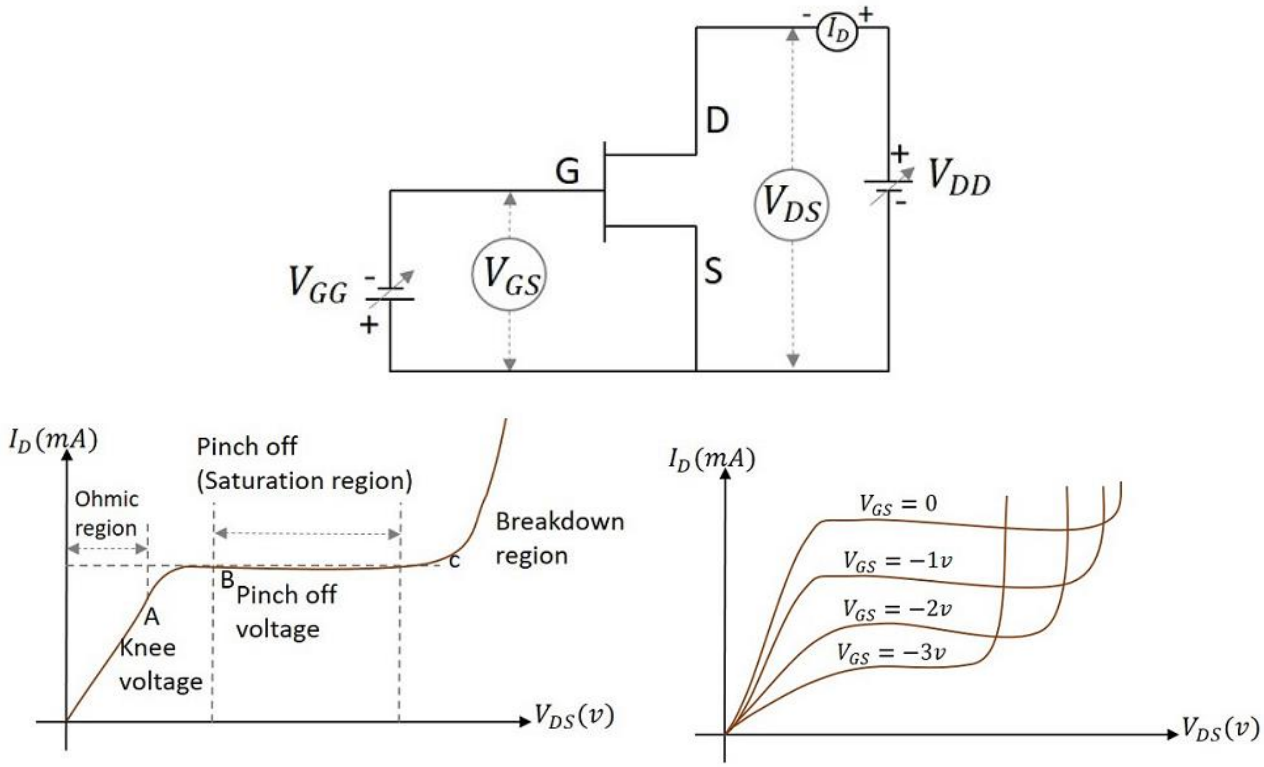


Fig.3.5:Drain characteristics of JFET

The gate terminals will be under reverse biased condition and as I_D increases, the depletion regions tend to constrict. This constriction is unequal in length making these regions come closer at drain and farther at drain, which leads to pinch off voltage. The pinch off voltage is defined as

the minimum drain to source voltage where the drain current approaches a constant value saturation value. The point at which this pinch off voltage occurs is called as Pinch off point, denoted as B.

As V_{DS} is further increased, the channel resistance also increases in such a way that I_D practically remains constant. The region BC is known as saturation region or amplifier region. All these along with the points A, B and C are plotted in the graph below

FET as an amplifier

A FET can work as an amplifier, in a way similar to that of a transistor. However gain of FET amplifier is comparatively lower than that of transistor. FET has some advantages over a junction transistor. The gate and source terminal is connected to the battery in such a way that gate terminal is connected to the negative terminal of the battery and source terminal is connected to the positive terminal of the battery. This is because we need to reverse bias the input circuitry of JFET.

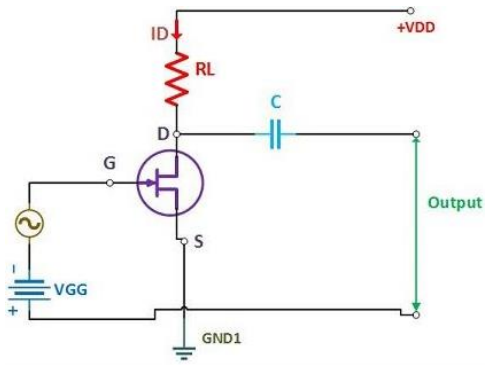


Fig.3.6:JFET as an Amplifier

The input signal which is weak in magnitude is applied by AC signal source. It is supplied as alternate positive, negative half cycles of AC. When the AC signal is applied to the input circuitry, it will start altering the gate to source voltage.

It will have two effects on the gate to source voltage, either it will reduce the magnitude of reverse biasing applied to the gate-source terminal, or it will increase the reverse biasing of the gate to the source terminal.

3.2 MOSFET

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor device that is widely used for switching purposes and for the amplification of electronic signals in electronic devices. A MOSFET is either a core or integrated circuit where it is designed and fabricated in a single chip because the device is available in very small sizes. The introduction of the MOSFET device has brought a change in the domain of switching in electronics.

3.2.1 Construction of MOSFET

A MOSFET is a four-terminal device having source(S), gate (G), drain (D) and body (B) terminals. In general, The body of the MOSFET is in connection with the source terminal thus forming a three-terminal device such as a field-effect transistor. MOSFET is generally considered as a transistor and employed in both the analog and digital circuits. This is the basic introduction to MOSFET. And the general structure of this device is as below :

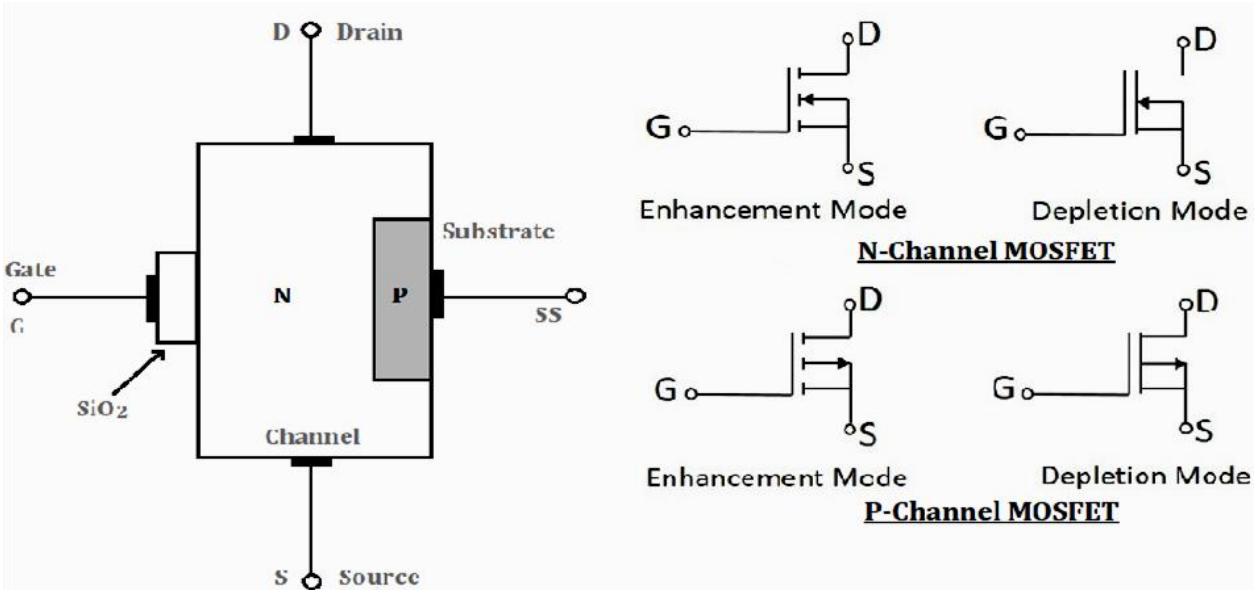


Fig.3.7: Construction &Symbol of MOSFET

From the above MOSFET structure, the functionality of MOSFET depends on the electrical variations happening in the channel width along with the flow of carriers (either holes or electrons). The charge carriers enter into the channel through the source terminal and exit via the drain.

The width of the channel is controlled by the voltage on an electrode which is called the gate and it is located in between the source and the drain. It is insulated from the channel near an extremely thin layer of metal oxide. The MOS capacity that exists in the device is the crucial section where the entire operation is across this.

A MOSFET can function in two ways

Depletion Mode

Enhancement Mode

Depletion Mode

When there is no voltage across the gate terminal, the channel shows its maximum conductance. Whereas when the voltage across the gate terminal is either positive or negative, then the channel conductivity decreases.

Enhancement Mode

When there is no voltage across the gate terminal, then the device does not conduct. When there is the maximum voltage across the gate terminal, then the device shows enhanced conductivity.

Operation or Working Principle of a MOSFET

The main principle of the MOSFET device is to be able to control the voltage and current flow between the source and drain terminals. It works almost like a switch and the functionality of the device is based on the MOS capacitor. The MOS capacitor is the main part of MOSFET.

The semiconductor surface at the below oxide layer which is located between the source and drain terminal can be inverted from p-type to n-type by the application of either a positive or negative gate voltages respectively. When we apply a repulsive force for the positive gate voltage, then the holes present beneath the oxide layer are pushed downward with the substrate.

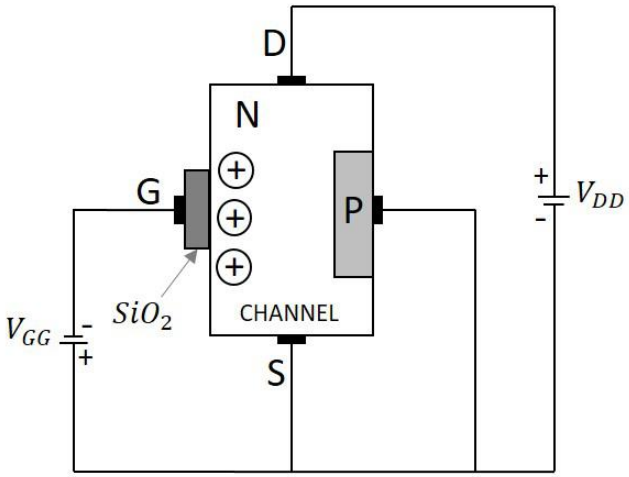


Fig.3.8: Operation or Working Principle of a MOSFET in depletion mode

The depletion region populated by the bound negative charges which are associated with the acceptor atoms. When electrons are reached, a channel is developed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Now, if a voltage is applied between the drain and source, the current flows freely between the source and drain and the gate voltage controls the electrons in the channel. Instead of the positive voltage, if we apply a negative voltage, a hole channel will be formed under the oxide layer.

P-Channel MOSFET

The P- channel MOSFET has a P- Channel region located in between the source and drain terminals. It is a four-terminal device having the terminals as gate, drain, source, and body. The drain and source are heavily doped p+ region and the body or substrate is of n-type. The flow of current is in the direction of positively charged holes.

When we apply the negative voltage with repulsive force at the gate terminal, then the electrons present under the oxide layer are pushed downwards into the substrate. The depletion region populated by the bound positive charges which are associated with the donor atoms. The negative gate voltage also attracts holes from the p+ source and drain region into the channel region.

N- Channel MOSFET

The N-Channel MOSFET has an N- channel region located in between the source and drain terminals. It is a four-terminal device having the terminals as gate, drain, source, body. In this type of Field Effect Transistor, the drain and source are heavily doped n+ region and the substrate or body are of P-type.

The current flow in this type of MOSFET happens because of negatively charged electrons. When we apply the positive voltage with repulsive force at the gate terminal then the holes present under the oxide layer are pushed downward into the substrate. The depletion region is populated by the bound negative charges which are associated with the acceptor atoms.

Upon the reach of electrons, the channel is formed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Now, if a voltage is applied between the drain and source the current flows freely between the source and drain and the gate voltage controls the electrons in the channel. Instead of positive voltage if we apply negative voltage then a hole channel will be formed under the oxide layer.

Enhancement Mode N Channel

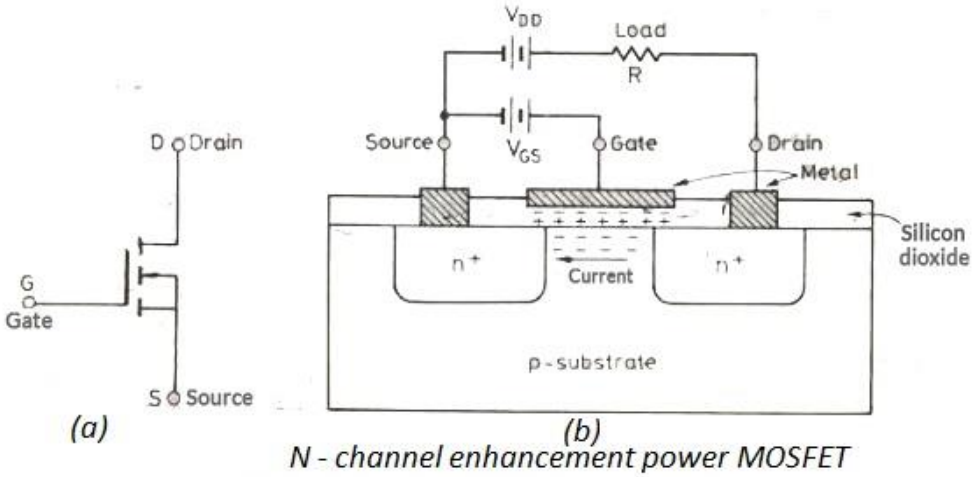


Fig.3.9:a) Circuit Symbol b) Basic Structure

MOSFET Regions of Operation

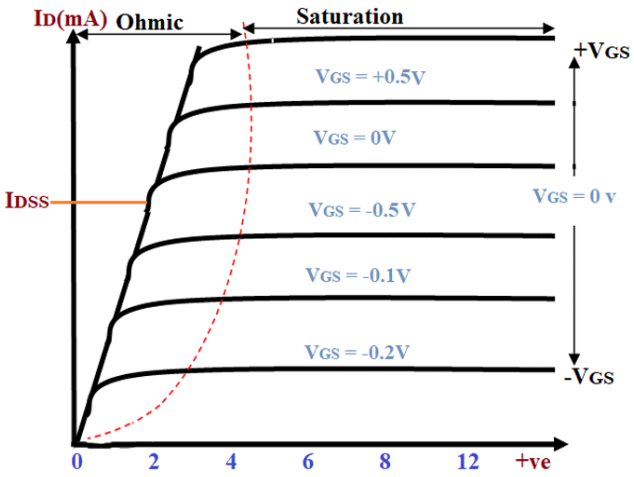
To the most general scenario, the operation of this device happens mainly in three regions and those are as follows:

Cut-off Region – It is the region where the device will be in the OFF condition and there zero amount of current flow through it. Here, the device functions as a basic switch and is so employed as when they are necessary to operate as electrical switches.

Saturation Region – In this region, the devices will have their drain to source current value as constant without considering the enhancement in the voltage across the drain to source. This happens only once when the voltage across the drain to source terminal increases more than the pinch-off voltage value. In this scenario, the device functions as a closed switch where a saturated level of current across the drain to source terminals flows. Due to this, the saturation region is selected when the devices are supposed to perform switching.

Linear/Ohmic Region – It is the region where the current across the drain to source terminal enhances with the increment in the voltage across the drain to source path. When the MOSFET devices function in this linear region, they perform amplifier functionality.

V-I characteristics of MOSFET



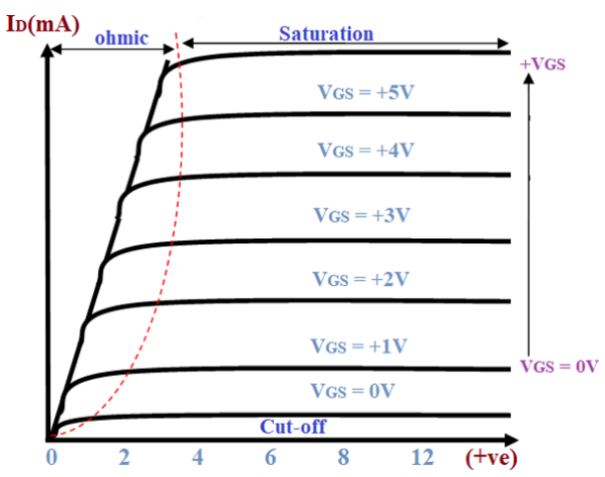


Fig.3.10: V-I characteristic of depletion mode MOSFETFig.3.11: V-I characteristic of enhencement mode MOSFET

Advantages

Few of the advantages are :

1. It generates enhanced efficiency even when functioning at minimal voltage levels.
2. There is no presence of gate current this creates more input impedance which further provides increased switching speed for the device.
3. These devices can function at minimal power levels and uses minimal current.

Disadvantages

- When these devices are functioned at overload voltage levels, it creates instability of the device
- As because the devices have a thin oxide layer, this may create damage to the device when stimulated by the electrostatic charges

Applications of MOSFET

The applications of MOSFET are

- Amplifiers made of MOSFET are extremely employed in extensive frequency applications
- The regulation for DC motors are provided by these devices
- As because these have enhanced switching speeds, it acts as perfect for the construction of chopper amplifiers
- Functions as a passive component for various electronic elements.
- MOSFET Application as Switch

3.3 Comparison of JFET, MOSFET and BJT

TERMS	**BJT**	**FET**	**MOSFET**
Device type	Current controlled	Voltage controlled	Voltage Controlled
Current flow	Bipolar	Unipolar	Unipolar
Terminals	Not interchangeable	Interchangeable	Interchangeable
Operational modes	No modes	Depletion mode only	Both Enhancement and Depletion modes
Input impedance	Low	High	Very high
Output resistance	Moderate	Moderate	Low
Operational speed	Low	Moderate	High
Noise	High	Low	Low
Thermal stability	Low	Better	High

COMPARISON BETWEEN JFET AND JUNCTION TRANSISTORS

Junction transistor is a bipolar device. It's operation depends on

1. Majority carriers as well as minority carriers while FET is a unipolar device. It's operation depends on the majority carrier only.

2. FET has high input impedance of the order of 100 Mega ohm to 10^9 Mega ohm while junction transistor has low input impedance.

3. Junction transistor is a current controlled device while FET is a voltage controlled device.

4.Junction transistor has a higher noise signal ratio than FET.

5. Thermal stability of FET is better than junction transistor.

6. Size of FET is smaller than junction transistors.
7. FETs have low transconductance, hence voltage gain is lower than junction transistors.

COMPARISON BETWEEN JFET AND MOSFET

MOSFET differs from JFET in two respects

1. The device operates with gate-to-channel voltages of both polarities. In one case, there is a depletion of mobile carriers in the channel and the channel conductance is reduced; this mode is analogous to the operation of a junction FET. In the case, there is an enhancement of mobile carriers in the channel and the channel conductance is increased. This mode is not permitted in a junction FET because it corresponds to forward bias on the gate junction.
2. The gate is physically isolated from the channel. Consequently, the gate current is exceedingly small (as little as 10^15 amperes) for both polarities of gate-to-channel voltage.

APPLICATIONS OF FET

FET can be used for almost all such applications for which a junction transistor is used. Such as single stage voltage amplifier, multi stage voltage amplifier, power amplifier, oscillators etc.

EXERCISE UNIT – 3

OBJECTIVE TYPE QUESTION

SECTION –A

Multiple Choice Questions:

Q. 1 The operation of a JFET involves

(a) a few of minority carriers (b) a flow of majority carriers

(c) recombination (d) negative resistance

Q. 2 A field effect transistor (FET)

(a) uses a high-concentration emitter junction

(b) uses a forward-biased P-N junction

(c) has a very high input resistance

(d) depends on minority-carrier flow

Q. 3 In a FET, the drain voltage above which there is no increase in drain current called:

(a) Break down voltage

(b) Pinch off voltage

(c) Critical voltage

(d) Threshold Voltage

Q. 4 A N-channel FET is never operated with positive gate voltage. This is because

(a) Gate to source current is to be avoided

(b) Drain current becomes high

(c) Drain current does not increase

(d) Drain current does not remain constant

Q. 5 In a JFET drain current will be maximum when V_{gs} is

(a) Equal to V_p (b) Positive

(c) negative (d) zero.

Q. 6 FET has

(a) Large input impedance (b) Large output impedance

(c) Large power gain (d) High voltage gain

Q. 7 A JEET can be cut off with the help of

(a) V_{ds} (b) V_{gs}

(c) V_{dg} (d)Drain supply

SHORT TYPE QUESTION

SECTION – B

Q. 1 Explain the structure of

(a) Field effect transistors

(b) Metal oxide semiconductor FET

Q. 2. Explain any three methods of manufacturing of transistors.

Q. 3. Draw a diagram showing the basic structure of an N-channel field effect transistor and show the biasing arrangement.

Q. 4. Draw a family of common source drain characteristics of N-channel JFET.

Q. 5. Define:

(a) the pinch off voltage,

(b) channel ohmic region,

(c) drain resistance,

Q. 6. Sketch the cross section on N-channel MOSFET in depletion mode and draw the symbols.

Q. 7. Compare a JFET and a bipolar transistor

Q. 8. Compare a JFET and a MOSFET.

LONG TYPE QUESTION

SECTION – C

Q. 1 Describe the main types of field effect transistors? Give the advantages of FETs over a bipolar junction?

Q. 2 Explain construction of Bipolar junction transistor .State its characteristics.

Answer of section A

1. (b) 2. (c) 3. (b) 4. (a) 5. (d) 6. (a) 7. (b)

UNIT IV: Digital Electronics

4.1 Distinction between analogue and digital signal.

Sr.No.	Analog Signals	Digital Signals
1.	Continuous signals	Discrete signals
2.	Represented by sine waves	Represented by Square waves
3.	Human voice, natural sound, analog electronic devices are a few examples	Computers, optical drives, and other electronic devices
4.	Continuous range of values	Discontinuous values
5.	Records sound waves as they are	Converts into a binary waveform
6.	Only used in analog devices	Suited for digital electronics like computers, mobiles and more

4.2 Number system

Decimal Number Decimal system is most familiar number system to the general public. It is base 10 which has only 10 symbols: 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9.

Binary Number

Binary is the simplest kind of number system that uses only two digits of 0 and 1 (i.e. value of base 2). Since digital electronics have only these two states (either 0 or 1), so binary number is most preferred in modern computer engineer, networking and communication specialists, and other professionals.

Octal Number System:-

Octal Number System is one the type of Number Representation techniques, in which there value of base is 8. That means there are only 8 symbols or possible digit values, there are 0, 1, 2, 3, 4, 5, 6, 7. It requires only 3 bits to represent value of any digit. Octal numbers are indicated by the addition of either an 0o prefix or an 8 suffix.

Position of every digit has a weight which is a power of 8. Each position in the Octal system is 8 times more significant than the previous position, that means numeric value of an octal number is determined by multiplying each digit of the number by the value of the position in which the digit appears and then adding the products. So, it is also a positional (or weighted) number system.

Representation of Octal Number:-

Each Octal number can be represented using only 3 bits, with each group of bits having a distich values between 000 (for 0) and 111 (for 7 = 4+2+1). The equivalent binary number of octal number are as given below –

Octal Digit Value	Binary Equivalent
0	000
1	001
2	010
3	011

4	100
5	101
6	110
7	111

Octal number system is similar to Hexadecimal number system. Octal number system provides convenient way of converting large binary numbers into more compact and smaller groups, however this octal number system is less popular.

Hexadecimal number system

Hexadecimal number is one of the number systems which has value is 16 and it has only 16 symbols – 0, 1, 2, 3, 4, 5, 6, 7, 8, 9 and A, B, C, D, E, F. Where A, B, C, D, E and F are single bit representations of decimal value 10, 11, 12, 13, 14 and 15 respectively.

Conversion

Conversion from decimal to binary

Conversion from hexadecimal to binary

Hexadecimal To Binary:-

Conversion from Hexadecimal to Decimal number system

There are various indirect or direct methods to convert a hexadecimal number into decimal number. In an indirect method, you need to convert a hexadecimal number into binary or octal number, then you can convert it into decimal number.

Example – Convert hexadecimal number F1 into decimal number.

First convert it into binary or octal number,

$= (F1)_{16}$

$= (1111\ 0001)_2$ or $(011\ 110\ 001)_2$

Because in binary, value of F and 1 are 1111 and 0001 respectively. Then convert it into decimal number multiplying power of its position of base.

= (1x27+1x26+1x25+1x24+0x23+0x22+0x21+1x20)10

or $(3\ 6\ 1)_8$

= (1x27+1x26+1x25+1x24+0x23+0x22+0x21+1x20)10 or (3x82+6x81+1x80)10

= (241)10However, there is a simple direct method to convert a hexadecimal number to decimal number. Since, there are only 16 digits (from 0 to 7 and A to F) in hexadecimal number system, so we can represent any digit of hexadecimal number system using only 4 bit as following below.

Hexa	0	1	2	3	4	5	6	7

Binary	0000	0001	0010	0011	0100	0101	0110	0111

Hexa	8	9	A=10	B=11	C=12	D=13	E=14	F=15
Binary	1000	1001	1010	1011	1100	1101	1110	1111

Hexadecimal number system provides convenient way of converting large binary numbers into more compact and smaller groups. These are weights of hexadecimal of respective position of hexadecimal (value of base is 16).

Most Significant Bit (MSB)	**Hexa Point**		**Least Significant Bit (LSB)**		
16^2	16^1	16^0	16^{-1}	16^{-2}	16^{-3}
256	16	1	1/16	1/256	1/4096

Since number numbers are type of positional number system. That means weight of the positions from right to left are as 16^0, 16^1, 16^2, $16^3$and so on. for the integer part and weight of the positions from left to right are as 16^{-1}, 16^{-2}, $16^{-3}$and so on. for the fractional part.

You can directly convert a hexadecimal number into decimal number using reverse method of decimal to hexadecimal number.

Assume any unsigned hexadecimal number is $h_nh_{(n-1)}$ ... $h_1h_0.h_{-1}h_{-2}$ ... $h_{(m-1)}h_m$. Then the decimal number is equal to the sum of hexadecimal digits (hn) times their power of 16 (16n), i.e.,

= $h_nh_{(n-1)}$ ... $h_1h_0.h_{-1}h_{-2}$ ... $h_{(m-1)}h_m$

= $h_nx16^n+h_{(n-1)}x16^{(n-1)}$+ ... +$h_1x16^1+h_0x16^0+h_{-1}x16^{-1}+h_{-2}x16^{-2}$+ ... +$h_{(m-1)}x16^{-(m-1)}+h_{-m}x16^{-m}$

This is simple algorithm where you have to multiply positional value of binary with their digit and get the sum of these steps.

Example-1 – Convert hexadecimal number ABCDEF into decimal number.

Since value of Symbols – A, B, C, D, E, F are 10, 11, 12, 13, 14, 15 respectively. Therefore

= $(10x165+11x164+12x163+13x162+14x161+15x160)_{10}$
equivalent decimal number is,

$(ABCDEF)_{16}$
= (10485760+720896+49152+3328+224+15)10
= (11259375)10 which is answer.
Conversion from binary to decimal
Conversion from binary to hexadecimal

Conversion from Binary to Hexadecimal number system

Hexadecimal number system provides convenient way of converting large binary numbers into more compact and smaller groups. There are various ways to convert a binary number into hexadecimal number. You can convert using direct methods or indirect methods. First, you need to convert a binary into other base system (e.g., into decimal, or into octal). Then you need to convert it hexadecimal number.

Most Significant Bit (MSB)	**Hexa Point**		**Least Significant Bit (LSB)**		
16^2	16^1	16^0	16^{-1}	16^{-2}	16^{-3}
256	16	1	1/16	1/256	1/4096

Since number numbers are type of positional number system. That means weight of the positions from right to left are as 16^0, 16^1, 16^2, $16^3$and so on. for the integer part and weight of the positions from left to right are as 16^{-1}, 16^{-2}, $16^{-3}$and so on. for the fractional part.

Example – Convert binary number 1101010 into hexadecimal number.

First convert this into decimal number:
$(1101010)_2$
$= 1x2^6+1x2^5+0x2^4+1x2^3+0x2^2+1x2^1+0x2^0$
$= 64+32+0+8+0+2+0$
$= (106)_{10}$
Then, convert it into hexadecimal number
$= (106)_{10}$
$= 6x16^1+10x16^0$
$= (6A)_{16}$ which is answer.

Binary addition

Rules of Binary Addition

Binary addition is much easier than the decimal addition when you remember the following tricks or rules. Using these rules, any binary number can be easily added. The four rules of binary addition are:

- 0 + 0 = 0
- 0 + 1 = 1
- 1 + 0 = 1
- 1 + 1 =10

How To Do Binary Addition?

Now, look at the example of the binary addition:101 + 101

Procedure for Binary Addition of Numbers:

101

(+) 101

- **Step 1:** First consider the 1's column, and add the one's column,(1+1) and it gives the result 10 as per the condition of binary addition.

- **Step 2:** Now, leave the 0 in the one's column and carry the value 1 to the 10's column.

1

101

(+) 101

————–

0

- **Step 3: Now add 10's place, 1+(0 + 0) = 1.** So, nothing carries to the 100's place and leave the value 1 in the 10's place

1

101

(+) 101

————-

10

Binary subtraction

In binary addition using 1's complement:-

A. Addition of a positive and a negative binary number

We discuss the following cases under this.

Case I: When the positive number has greater magnitude.

In this case addition of numbers is performed after taking 1's complement of the negative number and the end-around carry of the sum is added to the least significant bit.

complement: The following examples will illustrate this method in binary addition using 1's

1. Find the sum of the following binary numbers:

(i) + 1110 and - 1101

Solution:

+ 1 1 1 0 ⇒ 0 1 1 1 0

- 1 1 0 1 ⇒ 1 0 0 1 0 (taking 1's complement)

0 0 0 0 0

1 carry

0 0 0 0 1

Hence the required sum is + 0001.

(ii) + 1101 and - 1011

(Assume that the representation is in a signed 5-bit register).

Solution:

+ 1 1 0 1 ⇒ 0 1 1 0 1

- 1 0 1 1 ⇒ 1 0 1 0 0 (taking 1's complement)

0 0 0 0 1

1 carry

0 0 0 1 0

Hence the required sum is + 0010.

Case II: When the negative number has greater magnitude.

In this case the addition is carried in the same way as in case 1 but there will be non end-around carry. The sum is obtained by taking 1's complement of the magnitude bits of the result and it will be negative.

The following examples will illustrate this method in binary addition using 1's complement:

Find the sum of the following binary numbers represented in a sign-plus-magnitude 5-bit register:

(i) + 1010 and - 1100

Solution:

+ 1 0 1 0 ⇒ 0 1 0 1 0

- 1 1 0 0 ⇒ 1 0 0 1 1 (1's complement)

1 1 1 0 1

Hence the required sum is – 0010.

(ii) + 0011 and - 1101.

Solution:

+	0	0	1	1	⇒	0	0	0	1	1					
-	1	1	0	1	⇒	1	0	0	1	0	(1's	complement)			
	1	0				1				0					1

Hence the required sum is – 1010.

B. When the two numbers are negative

For the addition of two negative numbers 1's complements of both the numbers are to be taken and then added. In this case an end-around carry will always appear. This along with a carry from the MSB (i.e. the 4th bit in the case of sign-plus-magnitude 5-bit register) will generate a 1 in the sign bit. 1's complement of the magnitude bits of the result of addition will give the final sum.

The following examples will illustrate this method in binary addition using 1's complement:

Find the sum of the following negative numbers represented in a sign-plus-magnitude 5-bit register:

(i) -1010 and -0101

Solution:

-	1	0	1	0	⇒	1	0	1	0	1	(1's	complement)			
-	0	1	0	1	⇒	1	1	0	1	0	(1's	complement)			
	0	1				1				1					1
			1												carry
				1	0			0		0					0

1's complement of the magnitude bits of sum is 1111 and the sign bit is 1.

Hence the required sum is -1111.

(ii) -0110 and -0111.

Solution:

- 0 1 1 0 ⇒ 1 1 0 0 1 (1's complement)

- 0 1 1 1 ⇒ 1 1 0 0 0 (1's complement)

1 0 0 0 1

1 carry

1 0 0 1 0

1's complement of 0010 is 1101 and the sign bit is 1.

Hence the required sum is - 1101.

4.3 Logic gates

A logic gate is a building block of a digital circuit. Most logic gates have two inputs and one output and are based on Boolean algebra. At any given moment, every terminal is in one of the two binary conditions *false* (high) or *true* (low). False represents 0, and true represents 1. Depending on the type of logic gate being used and the combination of inputs, the binary output will differ. A logic gate can be thought of like a light switch, wherein one position the output is off—0, and in another, it is on—1. Logic gates are commonly used in integrated circuits (IC).

Basic logic gates

There are seven basic logic gates: AND, OR, XOR, NOT, NAND, NOR, and XNOR.

Definition, Symbols and Truth tables of AND, OR, NOT, NAND, NOR, XOR and XNOR of logic gates:-

AND gate

The *AND gate* is so named because, if 0 is called "false" and 1 is called "true," the gate acts in the same way as the logical "and" operator. The following illustration and table show the circuit symbol and logic combinations for an AND gate. (In the symbol, the input terminals are at left and the output terminal is at right.) The output is "true" when both inputs are "true." Otherwise, the output is "false." In other words, the output is 1 only when both inputs one AND two are 1.

AND gate

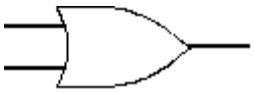
Input 1	Input 2	Output
0	0	0

0	1	0
1	0	0
1	1	1

Fig.4.1:Symbol and Truth Table of AND Gate

OR Gate:

The *OR gate* gets its name from the fact that it behaves after the fashion of the logical inclusive "or." The output is "true" if either or both of the inputs are "true." If both inputs are "false," then the output is "false." In other words, for the output to be 1, at least input one OR two must be 1.



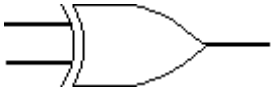
OR gate

Truth Table of OR gate:-

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	1

Fig.4.2:Symbol and Truth Table of OR Gate

XOR (exclusive-OR) gate The *XOR* (*exclusive-OR*) *gate* acts in the same way as the logical "either/or." The output is "true" if either, but not both, of the inputs are "true." The output is "false" if both inputs are "false" or if both inputs are "true." Another way of looking at this circuit is to observe that the output is 1 if the inputs are different, but 0 if the inputs are the same.



XOR gate

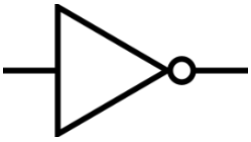
Truth Table of XOR gate:-

Input 1	Input 2	Output

0	0	0
0	1	1
1	0	1
1	1	0

Fig.4.3:Symbol and Truth Table of AND Gate

NOT gate A logical *inverter*, sometimes called a NOT gate to differentiate it from other types of electronic inverter devices, has only one input. It reverses the logic state. If the input is 1, then the output is 0. If the input is 0, then the output is**:**



NOT gate

Truth Table of NOT gate:-

Input	Output
1	0
0	1

Fig.4.4:Symbol and Truth Table of NOT Gate

NAND gate

The *NAND gate* operates as an AND gate followed by a NOT gate. It acts in the manner of the logical operation "and" followed by negation. The output is "false" if both inputs are "true." Otherwise, the output is "true."

NAND gate

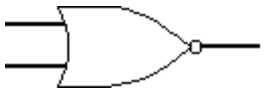
Truth Table of NAND gate:-

Input 1	Input 2	Output
0	0	1
0	1	1
1	0	1
1	1	0

4.5:Symbol and Truth Table of NAND Gate

NOR gate

The *NOR gate* is a combination OR gate followed by an inverter. Its output is "true" if both inputs are "false." Otherwise, the output is "false."



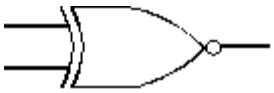
NOR gate

Input 1	Input 2	Output
0	0	1
0	1	0
1	0	0
1	1	0

4.6:Symbol and Truth Table of NOR Gate

XNOR (exclusive-NOR) gate

The *XNOR (exclusive-NOR) gate* is a combination XOR gate followed by an inverter. Its output is "true" if the inputs are the same, and "false" if the inputs are different.



XNOR gate

Input 1	Input 2	Output
0	0	1
0	1	0
1	0	0
1	1	1

4.7:Symbol and Truth Table of XNOR Gate

Using combinations of logic gates, complex operations can be performed. In theory, there is no limit to the number of gates that can be arrayed together in a single device. But in practice, there is a limit to the number of gates that can be packed into a given physical space. Arrays of logic gates are found in digital ICs. As IC technology advances, the required physical volume for each individual logic gate decreases and digital devices of the same or smaller size become capable of performing ever-more-complicated operations at ever-increasing speeds.

NAND and NOR as universal gates

NOR gate gives output 1 when all the applied inputs are 0 and gives output 0 when any of the input is 1. NAND gate gives output 0 when all the
inputs are 1, otherwise it gives output 1. NAND and NOR gates are called universal gates because we can make any gate with the use of NAND and NOR gate.

4.4 Gate realization with CMOS

CMOS

The term CMOS means complementary metal oxide semiconductor. This technology is most popular in design of chips for computers. It is broadly used integrated circuits This technology is being used in computer memories, cell phones, CPU. Microprocessor, micro computer chips , RAM,ROM and EPROM etc. It makes use of N channel as well as P channel devices.

CMOS technology has the advantage of low power dissipation. In static condition, there is no power dissipation as is there in case of BIPOLAR circuits. This results into better performance.

Working Principle:

Both N Type and P type semiconductors are used in CMOS technology to design a logic circuit. The same signal which turns on a P-Type device is used to turn off a N Type device. This gives the advantage of designing logic device with simple switches.

In CMOS logic gates, a collection of n type. MOSFETS is arranged in a pull down network between output and low voltage power supply rail. Both P-Type and N-Type transistors have their gates connected to same input. When P-Type MOSFET is ON, N-Type MOSFET is off and vice-versa, as shown in fig.4.8 given below:-

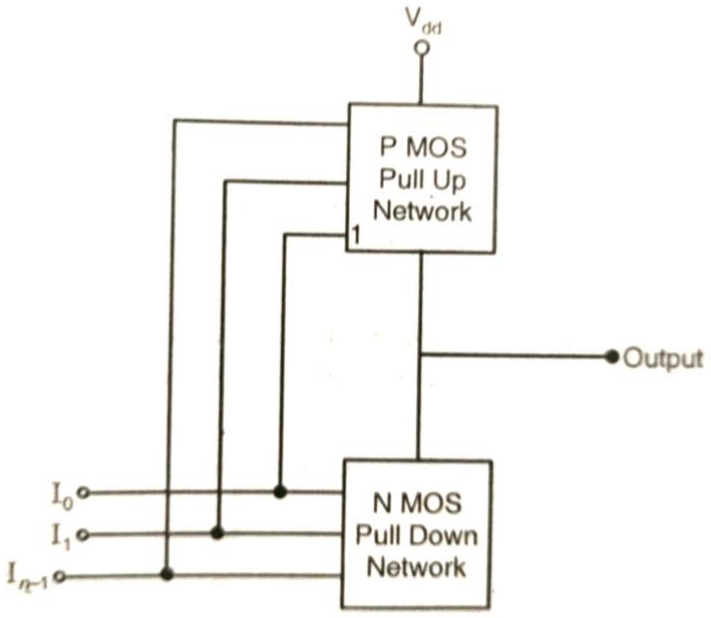


Fig.4.8 CMOS Logic gate using PULL up - pull down network

CMOS offers high speed, Low power dissipation, high margin of noise in either state and can be operated over wide range of source / input source.

CMOS Inverter

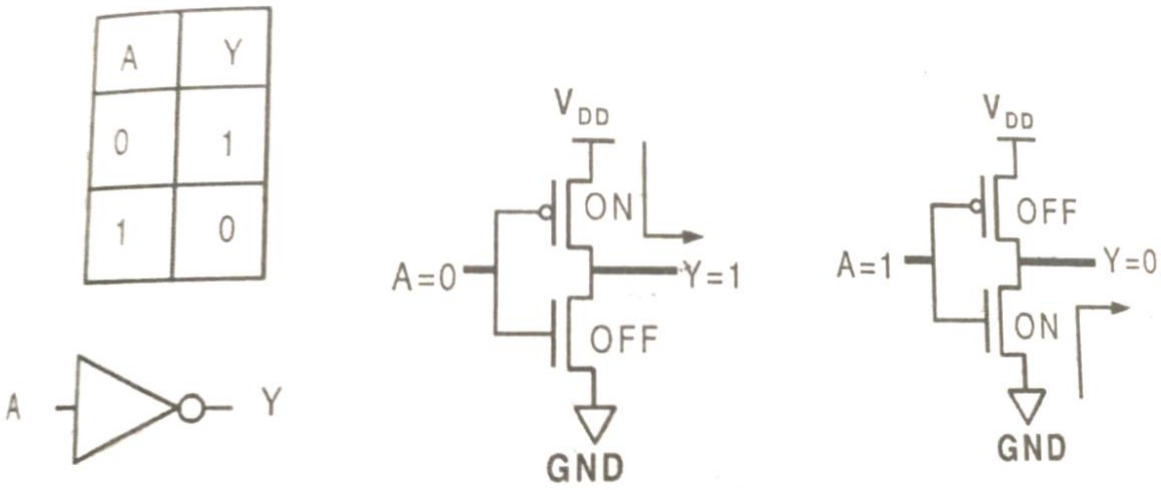


Fig. 4.9:CMOS inverter

The inverter circuit has a PMOS and NMOS FET. Both transistors are given input A as gate voltage NMOS has an input from V_{ss} (Ground) while PMOS transistor has an input from V_{DD}.
Output is taken from terminal Y. A high voltage applied as the input terminal A drives PMOS to open circuit and NMOS is switched off. Output will be pulled down to V_{ss}
On application of low voltage<V_{dd},0V. The NMOS is Switched OFF while PMOS is switched ON. Output is pulled down to V_{DD}.

CMOS Nand Gate

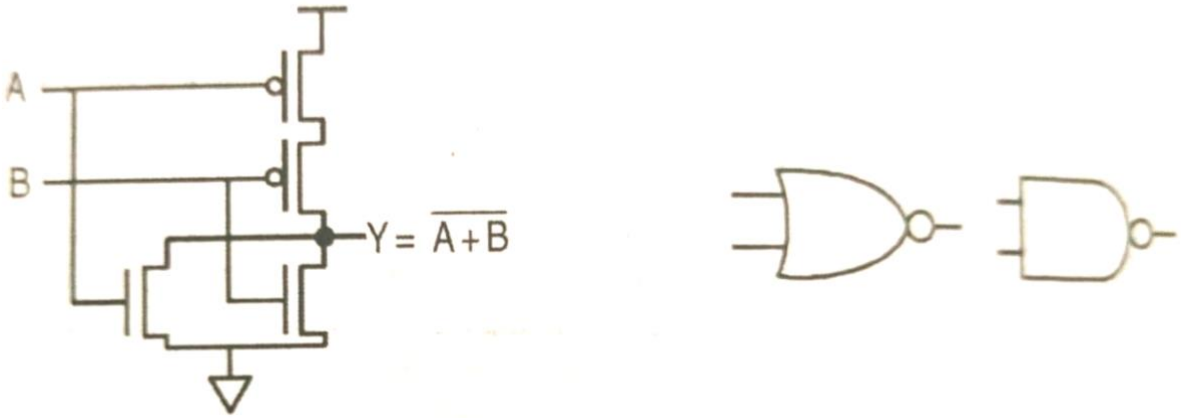
(a) 2-input NAND gate (b) NAND gate symbol

Fig.4.10.: CMOS Nand gate

A 2 input complementary MOS NAND gate is shown in fig. above. If any of the inputs A or B is logic 0, at least one of the NMOS transistor will be OFF, breaking the path from Y to Ground. At least one of the PMOS transistors will be ON, thereby creating a path from Y to V_{dd} Thus Output Y will be high.

lf both inputs are high, both NMOS transistors will be ON. While both PMOS transistors will be OFF. Output will be logic LOW. The truth table for a NAND gate is as below.

CMOS NOR Gate



(a) 2-input NOR gate schematic (b) NOR gate symbol

Fig.4.11: CMOS NOR gate

Fig.4.11 shows a 2 input NOR gate. 2 NMOS transistors are in parallel when either input is HIGH, the output is pulled LOW. PMOS transistors are in series when both inputs are low, output is pulled HIGH. The output is never left as floating.

CMOS Applications:

CMOS has almost raplaced NMOS and bipolar transistor in digital logic applications. CMOS technology is being used for digital IC designs in computer memories, CPU, Microprocessor designs, emory chip, and application specific integrated circuits (ASIC).

EXERCISE UNIT – 4

OBJECTIVE TYPE QUESTION

SECTION –A

Multiple Choice Questions:-

Q. 1 The base or radix of a binary number is

(i) 4 (ii) 3 (iii) 2 (iv) 0

Q. 2 A nibble represents

(i) Three bits (ii) Four bits (iii) Five bits (iv) Two bits

Q. 3 A byte represents

(i) Seven bits (ii) Eight bits (iii) Six bits (iv) Nine bits

Q. 4 Digits used in binary number system are

(i) 0 and1 (ii) 3 and 4 (iii) 1 and 2 (iv) 0 and 2

Q. 5 The base of a decimal number system is

(i) 8 (ii) 9 (iii) 10 (iv) 11

Q. 6 Distinct digits used in decimal number system are

(i) 0 to 7 (ii) 0 to 8 (ii) 0 to 9 (iv) 0 to 10

Q. 7 The radix of an octal number system is

(i) 8 (ii) 6 (iii) 2 (iv) 0

Q. 8 Distinct digits used in octal number system are

(i) 0 to 8 (ii) 0 to 7 (iii) 0 to 6 (iv) 0 to 9

Q. 9 The base of a hexadecimal number system is

(i) 15 (ii) 16 (iii) 14 (iv) 17

Q. 10 Distinct digits used in hexadecimal number system are

(i) 0 to 9 and A to G (ii) 0 to 8 and A to F

(iii) 0 to 9 and A to F (iv) 0 to 7 and A to F

Q. 11 A single digit in binary number system is called

(i) Bit (ii) base (iii) Nibble (iv) bright

Q. 12 How many bytes are there in the binary number 1110000111001100

(i)3 (i) 2 (ii)4 (iv) 8

Q. 13 A byte represents

(i) 3 nibble (ii) 2 nibble (iii) 8 nibble (iv) 4 nibble

Q. 14 $(110101)_2 = (.....)_{10}$

(i) 54 (ii) 53 (iii) 60 (iv) 63

Q. 15 $(13)_{10} = (....)_2$

(i) 1101 (ii) 1110 (iii) 1100 (iv) 1111

Q. 16 $(247)_{10} = (.....)_8$

(i)362 (ii) 367 (iii) 370 (iv) 365

Q. 17 $(1001110)_2 = (.....)_8$

(i) 114 (ii) 117 (iii) 116 (iv) 119

Q. 18 $(3A)_{16} = (.....)_{10}$

(i)55 (ii) 57 (iii) 56 (iv) 58

Q. 19 $(247)_8 = (...)_{16}$

(i)7A (ii) A7 (iii) 8A (iv) A9

Q. 20. How many nibbles are there in 10011110 number

(i) 3 (ii) 4 (iii) 2 (iv) 8

21. An OR gate has 5 inputs. How many input combinations are there in its truth table?

(i) 64 (ii) 32 (iii) 16 (iv) 128

22. Which of the following gates cannot be used as an inverter?

(i) NAND (ii) NOR (iii) XOR (iv) AND

23. The output of a gate is high when all the inputs are low. This is true for

(i) AND (ii) NAND (iii) OR (iv) NOR

24. Which gate is known as universal gate?

(i) AND (ii) NAND (iii) XOR (iv) XNOR

Q. 25. The output of AND gate is high when the applied inputs are A, B and C

(i) A=1, B= 0, C=1 (ii) A = 0, B= 1, C=1

(iii) A = 1, B= 1, C = 1 (iv) A = 1, B= 1, C = 0

Q. 26. The output of OR gate is high when the applied inputs are A, B, C

(i) A= 1, B=1, C=1 (ii) A = 0, B=0, C =0

(iii) A= 0, B=1, C=0 (iv) Both (i) and (iii)

Q. 27. For an AND gate

(i) Output is high if and only if all inputs are high

(ii) All low inputs produces high output

(iii)Output is low if and only if all inputs are high

(iv) Both (ii) and (iii)

Q. 28. The output of a gate is low when atleast one of its inputs is 1. This is true for

(i) NAND (ii) AND (iii) NOR (iv) OR

Q. 29. The output of a gate is 0 when atleast one of its inputs is 0. This is true for

(i)AND (ii) NAND (iii) NOR (iv) OR

Q. 30. The output of a gate is 1 if and only if all its inputs are 0. This is true for

(i) XOR (ii) AND (iii) NOR (iv) XNOR

Q. 31. Which of the following gates can be used as an inverter?

(i) AND (ii) NAND (iii) OR (iv) None of the above

Q. 32. The logical expression for XNOR gate is given by

(i)$A \oplus B$ (ii) $A \Theta B$ (iii) A. B (iv) A + B

Q. 33. The output of a two input gate is low if and only if its inputs are equal

This is true for

(i) XOR (ii) NAND (iii) NOR (iv) AND

Q. 34. The output of a two input gate is high if and only if its inputs are

unequal. This is true for

(i) OR (ii) XOR (iii) XNOR (iv) NAND

Q. 35. The output of a two input gate is high when both the inputs are of same values. This is true for

(i) XOR (ii) NAND (iii) XNOR (iv) NOR

SHORT TYPE QUESTION

SECTION – B

Q. 1 What do you mean by a number system? How many number systems are used in digital electronics?

Q. 2 Convert the following binary numbers into decimal numbers
(i) 1111 (ii) 10101010 (iii) 1111.011 (iv) 1011.0111

Q. 3 Convert the following decimal numbers into binary numbers
(i)89 (ii)36 (iii) 57 (iv) 55.25

Q. 4 Convert the following binary numbers into octal number system:
(i) 11100 (ii) 0111010 (iii) 011.011 (iv) 110.001

Q. 5 Convert the following octal numbers into binary numbers:
(i) 456 (ii) 342 (iii) 45.7 (iv) 64.5

Q. 6 Convert the following octal numbers into decimal numbers:
(i) 654 (ii) 234 (iii) 55.5 (iv) 32.4

Q. 7 Convert the following binary numbers into hexadecimal number system:
(i) 10101010111 (ii) 111110101100 (iii) 1010.0011 (iv) 111001.0010

Q. 8 Convert the following hexadecimal numbers into binary numbers:
(i) AF7 (ii) BCF5 (iii) 9A.23 (iv) AF.45

Q. 9 Convert the following hexadecimal numbers into decimal numbers:
(i) 7AF (ii) 9AD (iii) 7FFF

Q. 10 Convert the following hexadecimal numbers into octal numbers
(i) 2DAB (ii) A3B7 (iii) FA9 (iv) 9AD

Q. 11 Convert the following decimal numbers into hexadecimal numbers :
(i)786 (ii) 954 (iii) 3270

Q. 12 Convert the following octal numbers into hexadecimal numbers
(i) 3427 (ii) 2437 (iii) 1126

Q. 13 Add the following binary numbers :
(i) 101011 + 110010 (ii) 1010 +1101 (iii) 1101010 +0110110

Q. 14 Subtract the following binary numbers:
(i) 1100-10 (ii) 11001- 101 (iii) 1100- 1010

Q. 15 Multiply the following binary numbers:
(i) 1101x 101 (ii) 10101 x 100 (iii) 110110 x 0110

Q. 16 Divide the following binary numbers
(i) 11011 by 101 (ii) 1100 by 100 (iii) 111100 by 100

Q. 17 Explain the term logic gates.

Q. 18 Explain the terms positive logic and negative logic.

Q. 19 Draw the symbol, logical expression, truth table and pulsed operation of Not gate.

Q. 20 Draw the symbol, logical expression, truth table and pulsed operation of an OR gate.

Q. 21 Draw the symbol, logical expression, truth table and pulsed operation of

(i)AND gate (ii) NAND gate (iii) NOR gate

(iv) XOR gate (v) XNOR gate

Q. 22 Why NAND and NOR gates are known as universal gates?

Q. 23 Draw and explain pulsed operation of 3 input AND gate.

Q. 24 If an inverter is applied at the input of a NOR gate, what function it will perform?

Q. 25 Implement a NOR gate by using NAND gates only.

LONG TYPE QUESTION

SECTION – C

Q. 1 Describe the Gate realization with CMOS?

Q. 2 Write down definition, symbols and truth tables of AND, OR, NOT, NAND, NOR, XOR and XNOR of logic gates.

Q. 3 Explain in detail why NAND and NOR gates are known as universal gates.

Q. 4 Explain in detail the symbol, truth table, logical expression and pulsed operation of the following gates;

(i)3 Input NAND gate (ii) 3 Input OR gate

(iii) XNOR gate (iv) XOR gate

Q. 5 Explain working of CMOS inverter.

Q. 6 Explain working of CMOS NOR Gate.

Answer of section A

1. (iii)	2. (ii)	3. (ii)	4.(i)	5. (iii)	6.(iii)	7.(i)
8.(ii)	9. (ii)	10. (iii)	11.(i)	12. (ii)	13.(ii)	14.(ii)
15.(i)	16.(ii)	17.(iii)	18. (iv)	19. (ii)	20. (iii)	21. (ii)
22. (iv)	23. (ii)	24. (ii)	25. (ii)	26. (iv)	27. (i)	28.(iii)
29.(i)	30. (iii)	31. (ii)	32. (ii)	33.(i)	34.(ii)	35. (iii)

UNIT V: Sequential and Combinational Circuit

5.1 Sequential Circuits

Half adder

An arithmetic circuit that carries out summation of 2 inputs of one-bit is known as a half adder.

Everyone is familiar with basic addition technique in which when two bits are required to be added then, the addition begins with the rightmost column. As there is always a possibility of carry term to exists. The same rule is utilized in the operation of half adders.

The figure5.1 below represents the logic symbol for half adder:

Fig.5.1: Half adder

The figure clearly shows 2 applied inputs and 2 outputs for half adder. Out of the two, one output shows the summation while other shows carrry generated.

The fig.5.2 shown the logic circuit of half adder in order to understand its operation more clearly:

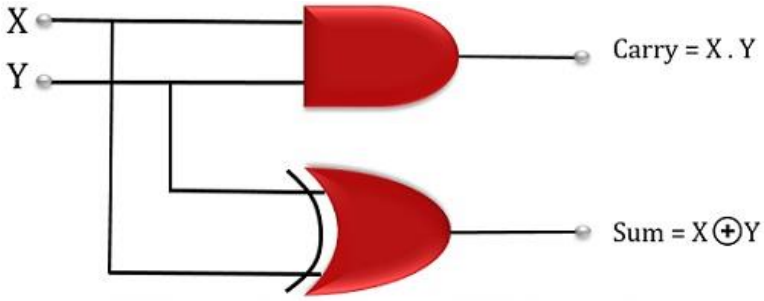


Fig.5.2 : Logic circuit of half adder

Here X and Y are the two inputs applied whereas S and C denotes the sum and carry bits. A half adder is composed of 1 AND gate and 1 XOR logic gate.

The summation bit generated by the half adder is represented by the XOR operation and the carry bit generated by the half adder is represented by the AND operation.

Fig.5.3 shown the truth table for half adder then we will summarize its operation:

Inputs		Outputs	
X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Fig.5.3 Truth table for half adder

Case 1: When both the applied inputs at the half adder is logic low i.e., 0 –
We know that summation of 0 and 0 will result in output 0 and in this case no any carry term is produced.
Case 2: When the first applied input is logic low i.e., 0 and second applied input is logic high i.e., 1 .
We know the addition of 0 and 1 will provide 1 as the sum but no any carry is generated in this case.
Case 3: When the first input is 1 and the second applied input is 0 –
Again the addition of 0 and 1 will generate 1 as the sum but no any carry bit will get generated.
Case 4: When both the applied inputs are logic high i.e., 1 –
The addition of 1 and 1 will generate 2 but in binary terms, we write 2 as 10. Thus, in this case, 0 will be the sum and 1 will become the carry bit.

Definition of Full Adder:-

Full adders are the arithmetic circuits that generate a summation of 3 inputs of one- bit.
The figure below represents the logic symbol of a full adder:

Fig.5.4: Full Adder

This figure 5.4 clearly shows the 3 inputs applied to the full adder and the 2 outputs. Here, also the one output shows the summation result and the other shows the carry bit generated.

The figure 5.6 represents the equivalent logic circuit for full adder:

This figure clearly shows the 3 inputs applied to the full adder and the 2 outputs. Here, also the one output shows the summation result and the other shows the carry bit generated.

The figure below represents the equivalent logic circuit for full adder:

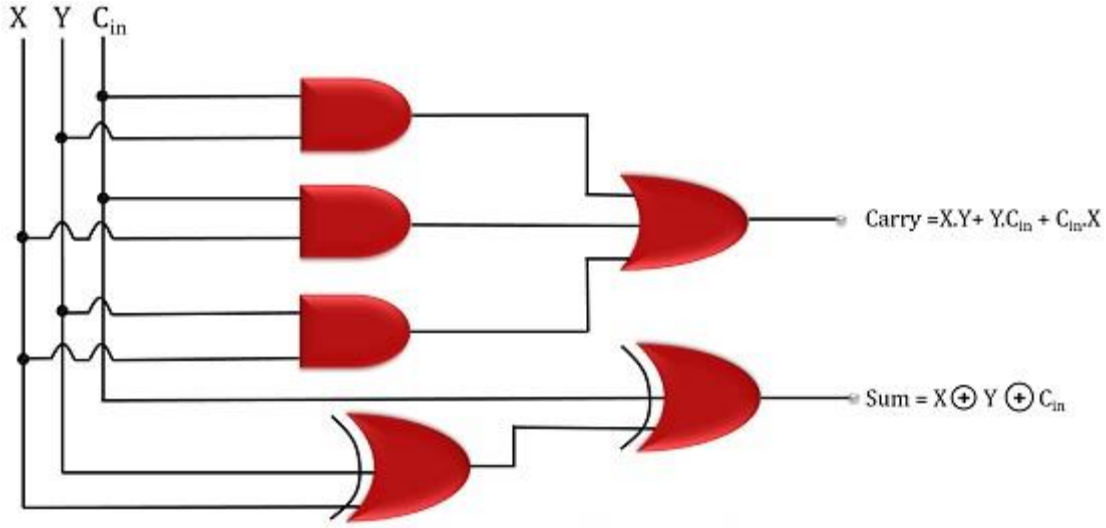


Figure 5.6 The equivalent logic circuit for full adder

Here, X, Y and C_{in} are the 3 inputs applied to the adder whereas S and C denotes the sum and carry generated.

Let us now analyze the truth table for full adder:

Inputs			Outputs	
X	Y	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth table for Full - Adder

We already know the fact that if only one of the inputs is logic high i.e., 1 and the rest are 0. Then, the sum generated will be 1 and the carry will be 0.But if out of 3, two inputs are logic high i.e., 1. Then its summation will generate 10 in binary forms representing 2. So, in this case, 0 is stored as the sum and 1 is stored as the carry. When all the 3 applied inputs are logic high i.e., 1 then, in this case, the sum generated will be 1 as well as the carry generated will also be 1.This is so because the addition of 1 and 1 give 0 as the sum and 1 as the carry this summed output 0 is then added with the last input 1. Thereby generating 1 as overall summation and 1 as the carry.

Multiplexer (Mux)

A multiplexer is a combinational logic circuit which has many inputs and single data output. The select lines decide which data input will be transferred to the output. The use of multiplexers make the design of digital circuits very simple because no simplification of Boolean expression are required.

This is also abbreviated as MUX. A MUX means many into one. So, multiplexer is a combinational circuit which has many inputs and only one output. The output is selected by the use of select lines. A multiplexer is also known as data selector because it accepts several data inputs and gives only one output which is selected by

the select lines. Figure shows the block diagram of a multiplexer.

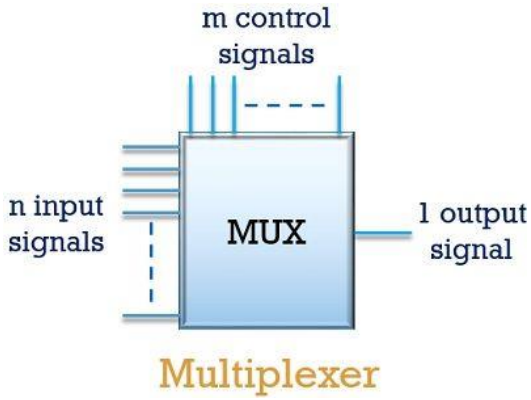


Fig.5.7 :-Multiplexer n:1

So, the block diagram shows that there are N data inputs and one output line. For

selecting one out of N inputs at the output, a set of m select lines is required. The relationship between data inputs lines (N) and select times (m) is given by

$2^m = N$

where N= no. of data inputs

m = number of select lines

it the number of inputs is 16, then the number of select lines can be found as

$16=2^m$

$2^4= 2^m$

So

m =4

Advantages:

The following are the advantages of using multiplexer:

1. Logic design is simplified because simplification of logic expressions is not required.
2. IC package count is reduced which reduces the cost of design.
3. A multiplexer is used for parallel to serial data conversion.
4.Multiplexer is also used for data routing because it can route data from one of the several source to one destination (output).

Demultiplexer (De-Mux)

A demultiplexer performs the reverse operation of a multiplexer. A Demux has one data input line and several output data lines. The select line inputs decide to which output is the data input is transferred.

DEMULTIPLEXER

Demultiplex means one into many. Demultiplexer is abbreviated as DEMUX. A DEMUX is a combinational logic circuit which performs the opposite operation to the MUX. It has single input and distributes this single input over several outputs. The select lines decide to which output the data input will be transmitted. Figure shows

the block diagram of a DEMUX:

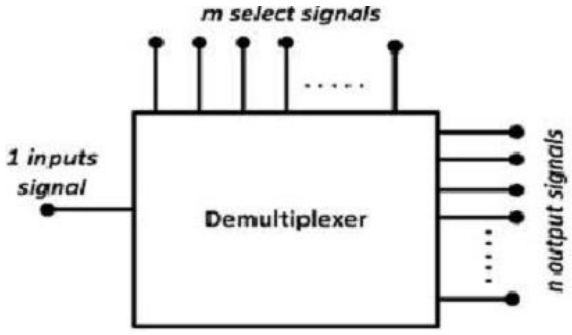


Fig.5.8: De-Mux 1:N

So, the block diagram of 1 : N DEMUX shows that there are N data outputs lines and m select lines and a single input data line. The relation between dataoutput lines and select lines is given by

$N = 2^m$

Where N=number of data outputs

m =number of select lines

Encoder:-

An encoder is a combinational circuit that performs the reverse operation of Decoder. It has maximum of 2^n input lines and 'n' output lines. It will produce a binary code equivalent to the input, which is active High. Therefore, the encoder encodes 2^n input lines with 'n' bits. It is optional to represent the enable signal in encoders.

4 to 2 Encoder:-

Let 4 to 2 Encoder has four inputs Y_3, Y_2, Y_1 & Y_0 and two outputs A_1 & A_0. The **block diagram** of 4 to 2 Encoder is shown in the following figure 5.9.

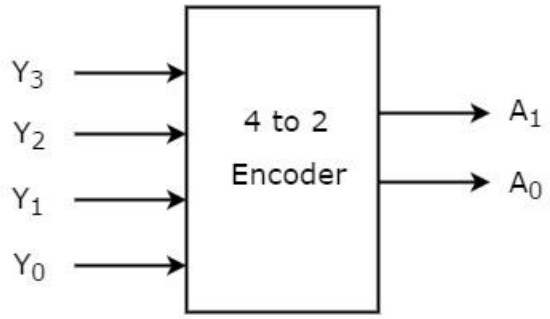


Fig.5.9: block diagram of 4 to 2 Encoder

At any time, only one of these 4 inputs can be '1' in order to get the respective binary code at the output. The **Truth table** of 4 to 2 encoder is shown below.

Inputs				**Outputs**	
Y_3	**Y_2**	**Y_1**	**Y_0**	**A_1**	**A_0**
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

From Truth table, we can write the **Boolean functions** for each output as

A1=Y3+Y2A1=Y3+Y2

A0=Y3+Y1A0=Y3+Y1

We can implement the above two Boolean functions by using two input OR gates. The **circuit diagram** of 4 to 2 encoder is shown in the following figure.

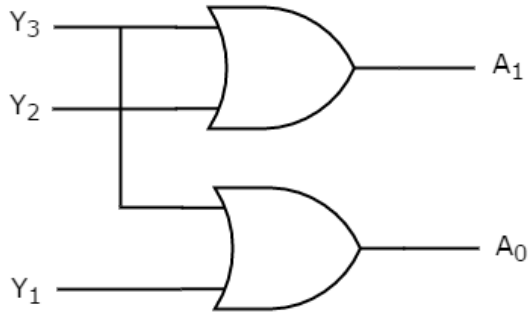


Fig.5.10: Circuit diagram of 4 to 2 encoder

The above circuit diagram contains two OR gates. These OR gates encode the four inputs with two bits.

Drawbacks of Encoder:-

Following are the drawbacks of normal encoder.

- There is an ambiguity, when all outputs of encoder are equal to zero. Because, it could be the code corresponding to the inputs, when only least significant input is one or when all inputs are zero.
- If more than one input is active High, then the encoder produces an output, which may not be the correct code. For **example**, if both Y_3 and Y_6 are '1', then the encoder produces 111 at the output. This is neither equivalent code corresponding to Y_3, when it is '1' nor the equivalent code corresponding to Y_6, when it is '1'.
- So, to overcome these difficulties, we should assign priorities to each input of encoder. Then, the output of encoder will be the binarybinary code corresponding to the active High inputss, which has higher priority. This encoder is called as priority encoder.

Decoder

A decoder is a logic circuit that accepts a set of inputs that represent a binary number and activates that output which corresponding to the input binary number. It is Multiple Input & Multiple Output device. Decoder is a combinational circuit that converts n lines of input into 2^n lines of output.

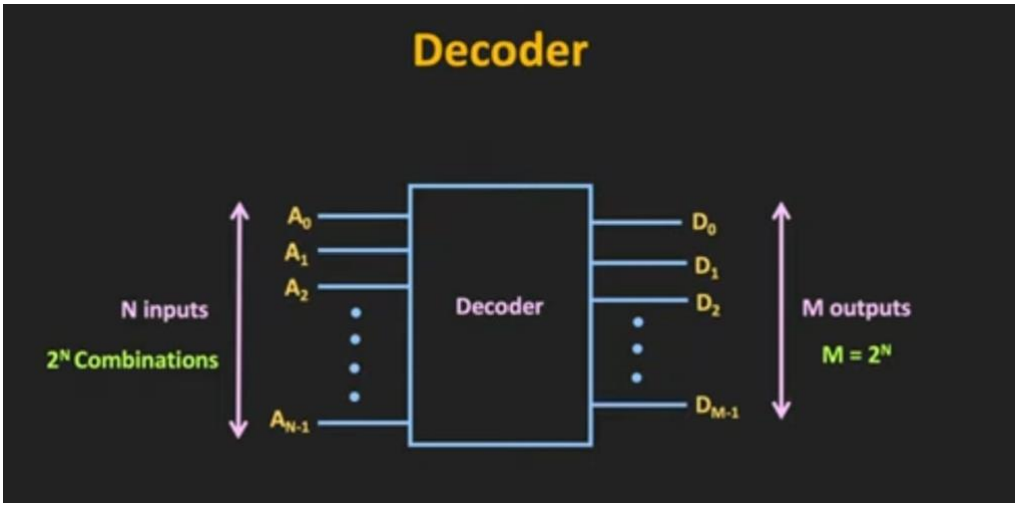


Fig.5.11: Decoder

Truth Table for decoder:-

Input		Output			
I_0	I_1	O_0	O_1	O_2	O_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Applications of decoders are converting binary code to other codes like:

1. Binary to octal
2. Binary to Hexadecimal
3. Binary to decimal

5.2 Combinational Circuits

Concept of latch

Latch:- latch is one kind of a logic circuit and it is also known as a bistable multivibrator. Because it has two stable states namely active high as well as active low. It works like a storage device by holding the data through a feedback lane. It stores 1-bit of data as long as the apparatus is activated. Once enable is declared then instantly latch can change the stored data. It constantly trials the inputs once enable signal is activated. The working of these circuits can be done in 2-states based on the enable signal being high or else low. When the latch circuit is the in an active high state, then both the i/ps are low. Similarly, when the latch circuit is then an active low state, then both the i/ps are high.

The latches can be classified into different types which include SR Latch, Gated S-R Latch, D latch, Gated D Latch, JK Latch, and T Latch.

LATCH VERSUS FLIP FLOP

LATCH	FLIP FLOP
Building blocks of sequential circuits, built using logic gates	Building blocks of sequential circuits, built using latches
Checks input continuously and changes output correspondingly	Checks input continuously and changes the output in a corresponding manner only with the clock signal
Sensitive to the input switch and is capable of transmitting data as long as the switch is in an on state	Sensitive to the clock signal, and the output will not change until a change occurs in the input clock signal
Work with only binary inputs	Works with binary inputs as well as the clock signal
Level triggered as the output will only change with the change in the binary level	Edge triggered as the output will change based on the positive edge or the negative edge of the clock signal
Cannot be used as a register	Can be used as a register
Asynchronous	Synchronous
No clock signal	Has a clock signal

Both latches and flip-flops are bistable devices used to store the one bit information. The main difference between two is the method of changing the output state.

Both latch and flip-flop have two stable state. They are capable to remain in one state, this may be set state or reset state. In this flip-flop state is changed on the application of triggering pulse. The pulse have two edge and each of flip-flop must be triggered one of them. So flip-flop may be of positive edge triggering device or negative edge triggering device.

Simple edge triggered flip-flop have problem of race around condition in which the output of flip-flop is unpredictable during one clock pulse. To avoid this type of problem, master slave flip-flop is used in this flip-flop if data are entered on the +ve edge of the clock then data must be retrieved on the negative edge of the clock. So, in this both edge of the clock pulse is used and problem of race around condition is removed.

Flip Flops (S-R, D, J-K, T types)

S-R Flip Flop

The SR flip-flop is also named as RS flip flop. When both the inputs of the SR flip-flop are high, then the indeterminate state is theirs. In other programming environments, it is required to assign determinate outputs to all flip flop conditions. Hence, RS and SR flip-flops were designed. The clocked SR flip-flop is shown below.

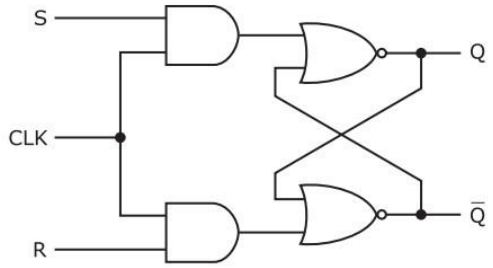
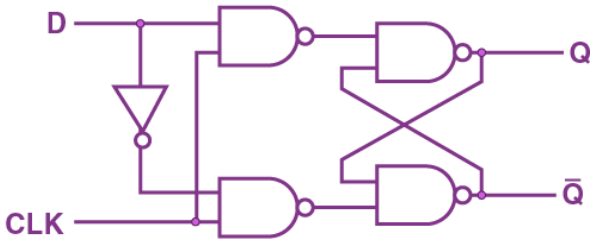


Fig.5.12: Clocked SR flip-flop

SR Flip-Flop Truth Table				
Clock	**S**	**R**	**Q_{n+1}**	
0	X	X	Qn	X
1	0	0	Qn	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	X	Invalid

Fig.5.13:SR Flip Flop Truth Table

D Flip Flop : Delay Flip Flop

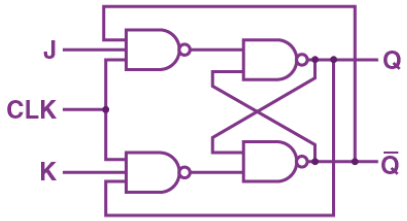


Truth Table

Q	D	$Q_{(t+1)}$
0	0	0
0	1	1
1	0	0
1	1	1

Fig.5.14: D Flip Flop with Truth Table

J-K Flip Flop:- The SR Flip Flop with Inverse feedback is Called J-K Flip Flop. The Fig.5.15 Shows the JK flip flop with truth table.



Truth Table

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

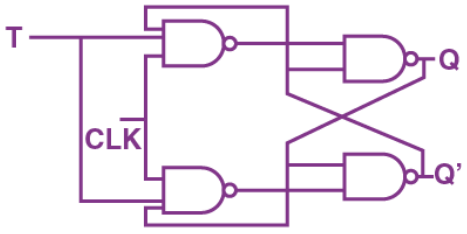
Fig.5.15: JK flip flop with truth table

Race-Around Condition

When both J and K inputs are high, then in the presence of clock pulse, output toggle i.e. if Q = 0 then Qn+1 = 1 or if Q =1 then Qn+1 0. This output changes occurs after a time interval t equal to propagation delay through two NAND gates in series. Since output is feedback to the input, so after t time from start of pulse, input condition changes. If the pulse is still there after t time interval, output again toggles & this condition continues. At the end of clock pulse, value of Q is uncertain. This condition is called Race-around condition. lt can be avoided if At is greater than pulse width duration but it is very difficult.

T Flip Flop:- Toggle Flip Flop

The fig.5.16 shows the toggle flip flop with truth table.



Truth Table

T	Q_N	Q_{N+1}
0	0	0
0	1	1
1	0	1
1	1	0

Fig.5.16 Toggle flip flop with truth table.

Basic concept of shift registers

In **Serial In Parallel Out (SIPO) shift registers**, the data is stored into the register serially while it is retrieved from it in parallel-fashion. Figure5.17 shows an n-bit synchronous **SIPO shift register** sensitive to positive edge of the clock pulse. Here the data word which is to be stored (Data in) is fed serially at the input of the first flip-flop (D_1 of FF_1). It is also seen that the inputs of all other flip-flops (except the first flip-flop FF_1) are driven by the outputs of the preceding ones say for example, the input of FF_2 is driven by the output of FF_1. In this kind of shift register, the data stored within the register is obtained as a parallel-output data word (Data out) at the individual output pins of the flip-flops (Q_1 to Q_n).

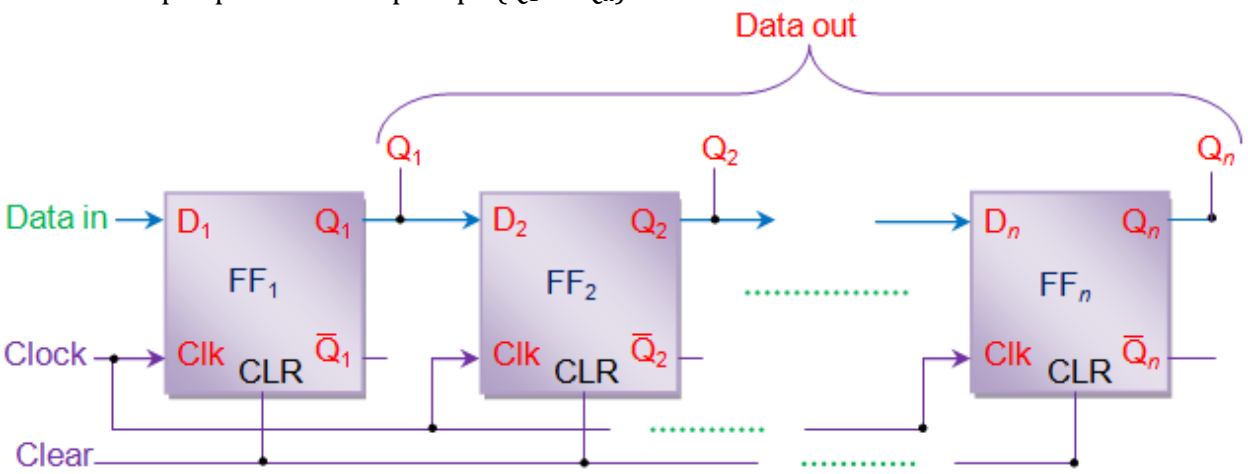


Fig.5.17: n Bit SIPO Right Shift Shift Register

In general, the register contents are cleared by applying high on the clear pins of all the flip-flops at the initial stage. After this, the first bit, B_1 of the input data word is fed at the D_1 pin of FF_1. This bit (B_1) will enter into FF_1, get stored and thereby appears at its output Q_1 on the appearance of first leading edge of the clock. Further at the second clock tick, the bit B_1 right-shifts and gets stored into FF_2 while appearing at its output pin Q_2 while a new bit, B_2 enters into FF_1. Similarly at each clock tick the data within the register moves towards right by a single bit while a new bit of the input word enters into the register. Meanwhile one can extract the bits stored within the register in parallel-fashion at the individual flip-flop outputs.

Analyzing on the same grounds, one can note that the n-bit input data word is obtained as an n-bit output data word from the shift register at the rising edge of the n^{th} clock pulse. This working of the shift-register can be summarized as in Table I and the corresponding wave forms are given by Figure 5.18.

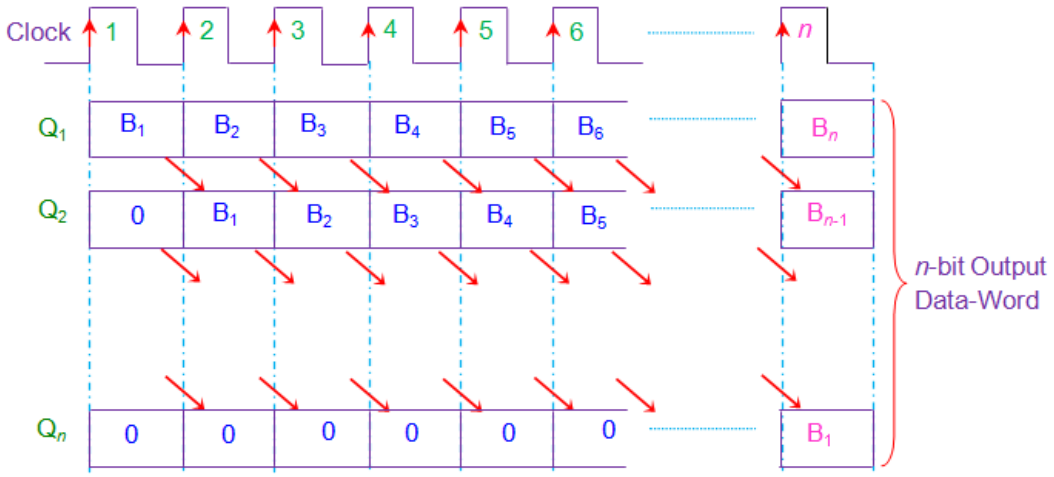


Fig.5.18: Output Waveform of n-bit Right Shift SIPO Shift Register

In the right-shift SIPO shift-register, data bits shift from left to right for each clock tick. However if the data bits are made to shift from right to left in the same design, one gets a left-shift SIPO shift-register as shown by Figure 3. Nevertheless the basic working principle remains the same except the fact that now B_n down to B_1 is stored in Q_n down to Q_1 i.e. $Q_1 = B_1$, $Q_2 = B_2$ … $Q_n = B_n$ at the n^{th} clock tick.

Serial In Serial Out (SISO) shift registers are a kind of shift registers where both data loading as well as data retrieval to/from the shift register occurs in serial-mode. Figure 5.19 shows a n-bit synchronous **SISO shift register** sensitive to positive edge of the clock pulse. Here the data word which is to be stored is fed bit-by-bit at the input of the first flip-flop. Further it is seen that the inputs of all other flip-flops (except the first flip-flop FF_1) are driven by the outputs of the preceding ones say for example, the input of FF_2 is driven by the output of FF_1. At last the data stored within the register is obtained at the output pin of the n^{th} flip-flop in serial-fashion.

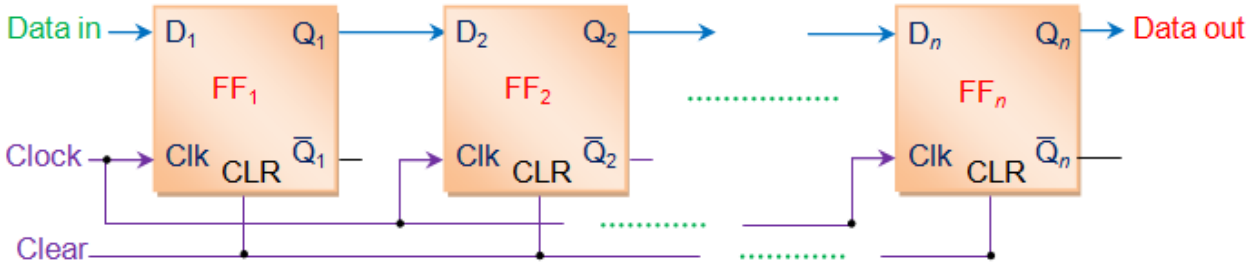


Fig.5.19: n Bit SISO Right Shift Shift Register

Initially all the flip-flops in the register are cleared by applying high on their clear pins. Next the input data word is fed serially to FF_1.

This causes the bit appearing at the D_1 pin (B_1) to be stored into FF_1 as soon as the first leading edge of the clock appears. Further at the second clock tick, B_1 gets stored into FF_2while a new bit enters into FF_1 (B_2).
This kind of shift in data bits continues for every rising edge of the clock pulse. This indicates that for every single clock pulse the data within the register moves towards right by a single bit. Thus the design shown in Figure 5.19 is regarded as a right-shift **SISO shift register**. Following the data transmission as explained, one can note that the first bit of an input word appears at the output of n^{th} flip-flop for the n^{th} clock tick. On applying further clock cycles, one gets the next successive bits of the input data word as the serial output (Table I). The waveforms pertaining to the same are shown by Figure 5.20.

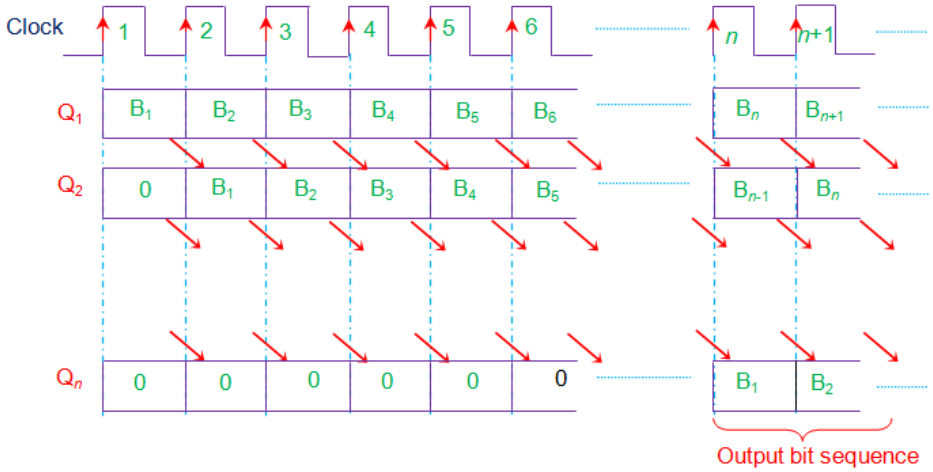


Fig.5.20: Output Waveform of n-bit Right Shift SISO Shift Register

Similar to the right-shift SISO shift-register shown, there can exist a left-shift **SISO shift-register** also . However the working principle remains the same except the fact that the data movement will be from right to left.

Parallel in-Serial out (PISO) Shift Register:-

This shift register allows parallel input and generates a serial output, so this is known as Parallel in Serial out (PISO) Shift Register.

The Parallel in Serial out (PISO) Shift Register circuit is shown above. This circuit can be built with four D-flip-flops, where the CLK signal is connected directly to all the FFs. However, the input data is connected separately to every FF using a **multiplexer** at every FF's input.

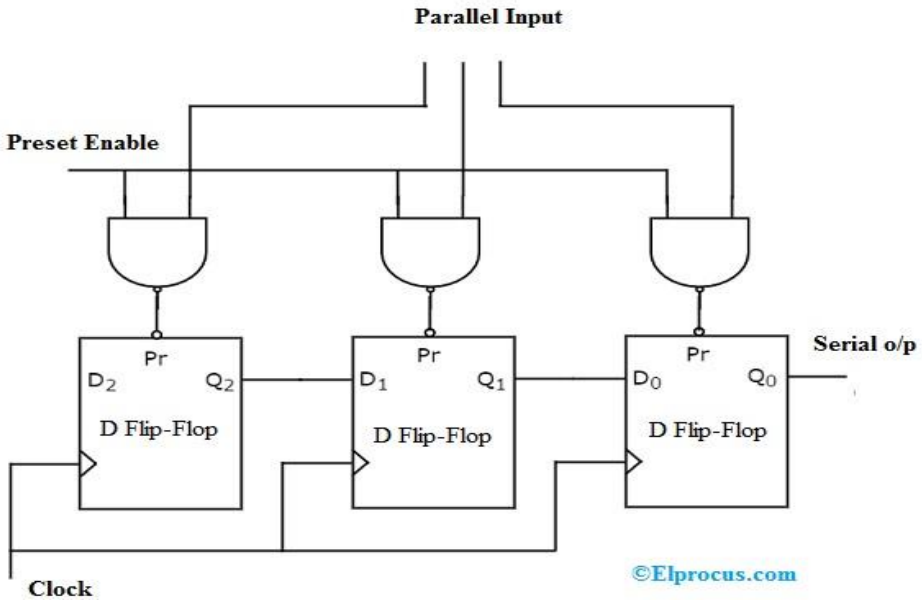


Fig.5.21: PISO Shift Register

The earlier FF output, as well as parallel data input, is connected toward the multiplexer's input & multiplexer's output can be connected to the second flip flop. Once the same CLK signal is given

to every flip flop, then all the flip flops will be synchronous with each other. The applications of these registers include converting parallel data to the serial data.

Parallel in-Parallel out (PIPO) Shift Register:-

The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and also produces a parallel output is known as Parallel-In parallel-Out shift register. The logic circuit given below shows a parallel in parallel out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal and clock signals are connected to all the 4 flip flops. In this type of register, there is no interconnection between the individual flip-flops as no data serial shifting is necessary. Here the data is given as input individually for every flip-flop, as well as the output is also received separately from every flip flop.

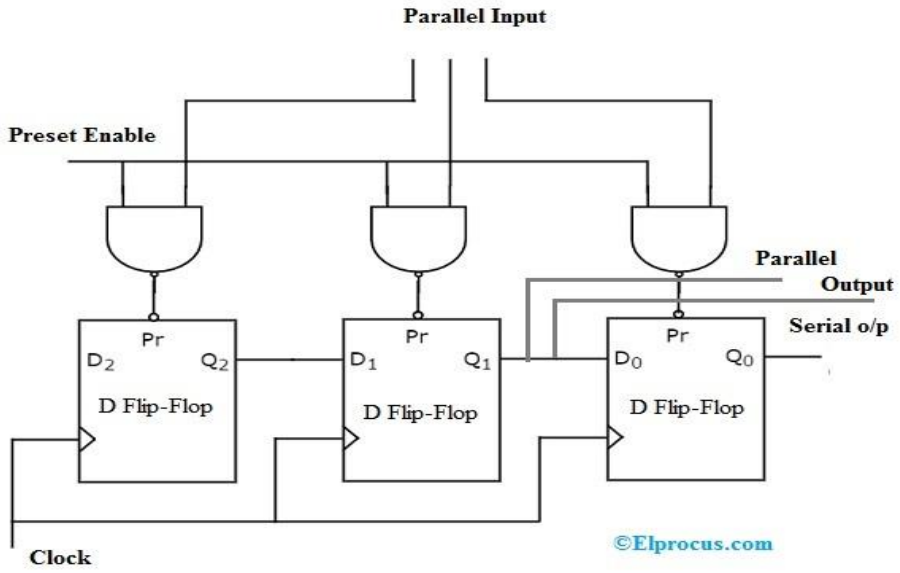


Fig.5.22: PIPO Shift Register

A PIPO (Parallel in Parallel out) shift register can be utilized like a temporary storage device, similar to SISO Shift register, and it performs like a delay element.

COUNTER:-

S.NO	SYNCHRONOUS COUNTER	ASYNCHRONOUS COUNTER
1.	In synchronous counter, all flip flops are triggered with same clock simultaneously.	In asynchronous counter, different flip flops are triggered with different clock, not simultaneously.

2.	Synchronous Counter is faster than asynchronous counter in operation.	Asynchronous Counter is slower than synchronous counter in operation.
3.	Synchronous Counter does not produce any decoding errors.	Asynchronous Counter produces decoding error.
4.	Synchronous Counter is also called Parallel Counter.	Asynchronous Counter is also called Serial Counter.
5.	Synchronous Counter designing as well implementation are complex due to increasing the number of states.	Asynchronous Counter designing as well as implementation is very easy.
6.	Synchronous Counter will operate in any desired count sequence.	Asynchronous Counter will operate only in fixed count sequence (UP/DOWN).
7.	Synchronous Counter examples are: Ring counter, Johnson counter.	Asynchronous Counter examples are: Ripple UP counter, Ripple DOWN counter.

Ripple counter –

A n-bit ripple counter can count up to 2n states. It is also known as MOD n counter. It is known as ripple counter because of the way the clock pulse ripples its way through the flip-flops. Some of the features of ripple counter are:

1. It is an asynchronous counter.
2. Different flip-flops are used with a different clock pulse.
3. All the flip-flops are used in toggle mode.
4. Only one flip-flop is applied with an external clock pulse and another flip-flop clock is obtained from the output of the previous flip-flop.
5. The flip-flop applied with external clock pulse act as LSB (Least Significant Bit) in the counting sequence.

A counter may be an up counter that counts upwards or can be a down counter that counts downwards or can do both i.e.count up as well as count downwards depending on the input control. The sequence of counting usually gets repeated after a limit. When counting up, for n-bit counter the count sequence goes from 000, 001, 010, … 110, 111, 000, 001, … etc. When counting down the count sequence goes in the opposite manner: 111, 110, … 010, 001, 000, 111, 110, … etc.

A 3-bit Ripple counter using JK flip-flop:-

In the circuit shown in above figure, Q0(LSB) will toggle for every clock pulse because JK flip-flop works in toggle mode when both J and K are applied 1, 1 or high input.

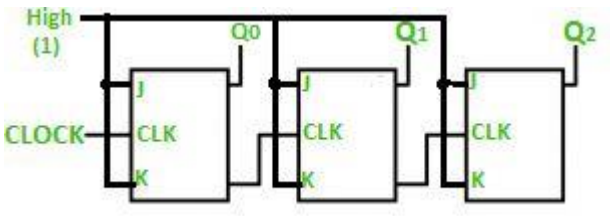


Fig.:5.23: 3-bit Ripple counter using JK flip-flop

The following counter will toggle when the previous one changes from 1 to 0

Truth Table for 3-bit Ripple counter:-

Counter State	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

The 3-bit ripple counter used in the circuit above has eight different states, each one of which represents a count value. Similarly, a counter having n flip-flops can have a maximum of 2 to the power n states. The number of states that a counter owns is known as its mod (modulo) number. Hence a 3-bit counter is a mod-8 counter.

A mod-n counter may also be described as a divide-by-n counter. This is because the most significant flip-flop (the furthest flip-flop from the original clock pulse) produces one pulse for every n pulses at the clock input of the least significant flip-flop (the one triggers by the clock pulse). Thus, the above counter is an example of a divide-by-4 counter.

Timing diagram – Let us assume that the clock is negative edge triggered so above counter will act as an up counter because the clock is negative edge triggered and output is taken from Q.

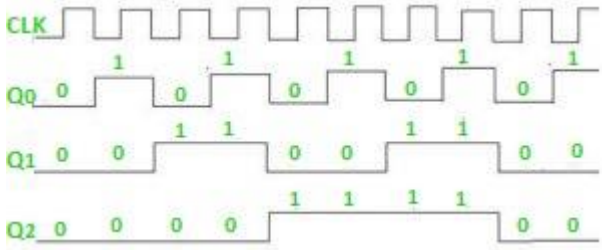


Fig.5.24:Timing Diagram3-bit Ripple counter

Counters are used very frequently to divide clock frequencies and their uses mainly involve in digital clocks and in multiplexing. The widely known example of the counter is parallel to serial data conversion logic.

5.3 A/D and D/A Converters

Basic concept of A/D converters, Types of Analog to Digital Converters

Some of the types of analog to digital converters include:

- Dual Slope A/D Converter
- Flash A/D Converter
- Successive Approximation A/D Converter

Dual Slope A/D Converter:-

In this type of ADC converter comparison voltage is generated by using an integrator circuit which is formed by a resistor, capacitor and operational_amplifier combination. By the set value

of V_{ref}, this integrator generates a sawtooth waveform on its output from zero to the value V_{ref}. When the integrator waveform is started correspondingly counter starts counting from 0 to 2^{n-1} where n is the number of bits of ADC.

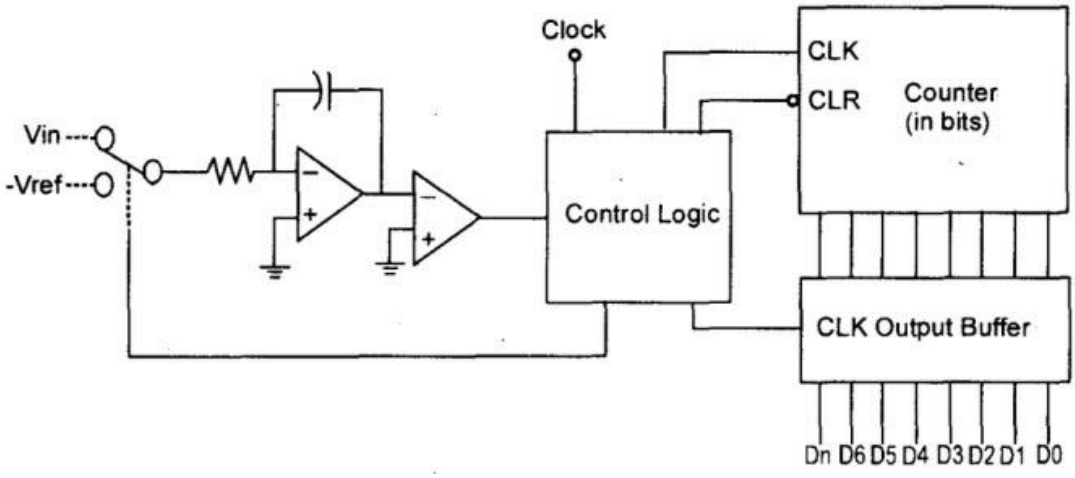


Fig.5.25: Dual Slope A/D Converter

When the input voltage V_{in} equal to the voltage of the waveform, then control circuit captures the counter value which is the digital value of corresponding analog input value. This Dual slope ADC is relatively medium cost and slow speed device.

Successive Approximation A/D Converter

The SAR ADC a most modern ADC IC and much faster than dual slope and flash ADCs since it uses a digital logic that converges the analog input voltage to the closest value. This circuit consists of a comparator, output latches, successive approximation register (SAR) and D/A converter.

At the start, SAR is reset and as the LOW to HIGH transition is introduced, the MSB of the SAR is set. Then this output is given to the D/A converter that produces an analog equivalent of the MSB, further it is compared with the analog input Vin. If comparator output is LOW, then MSB will be cleared by the SAR, otherwise the

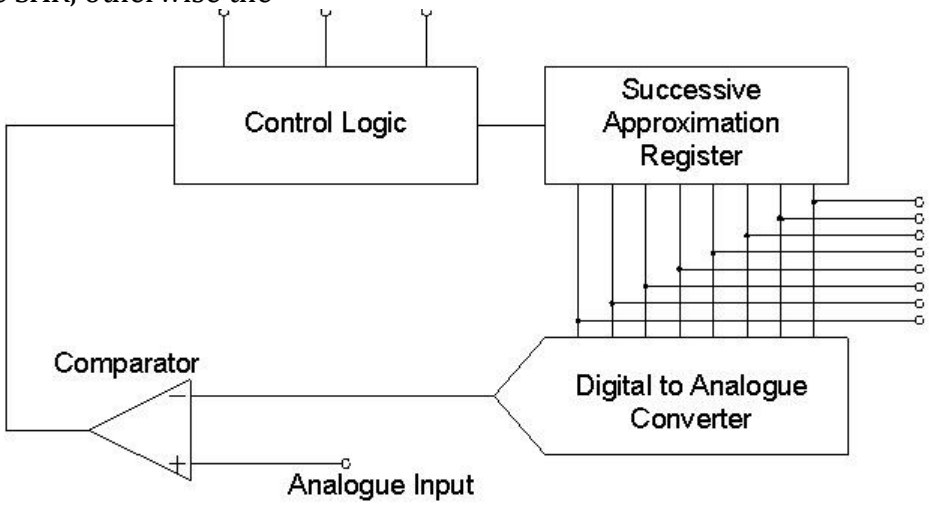


Fig.:5.26: Successive Approximation A/D Converter

MSB will be set to the next position. This process continues till all the bits are tried and after Q0, the SAR makes the parallel output lines to contain valid data.

This is about the ADC converter and its types. For easier understanding only few ADC converters are discussed in this article. We hope this furnished content is more informative to readers. Any further queries, doubts and technical help on this topic you can comment below.

Principles of ADC (Analog to Digital Conversion):-

Principles of ADC – The input signal is compared with an internally generated voltage which is increased in steps starting from zero. The number of steps needed to reach the full compensation is counted. A simple compensation type is the staircase ramp.

The Staircase Ramp

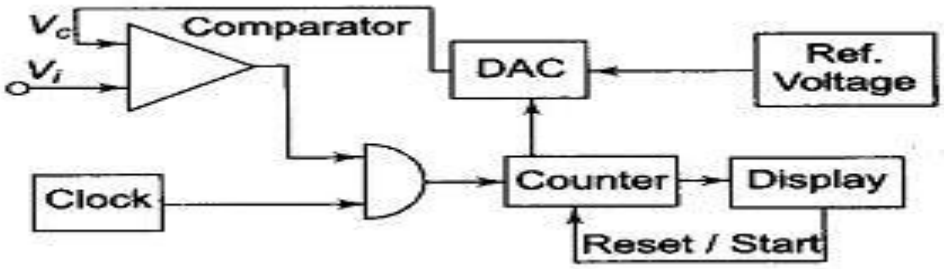


Fig.5.27: Block Diagram of a staircase Ramp Type

The basic block diagram is shown in Fig5.27. The basic principle is that the input signal V_i is compared with an internal staircase voltage, V_c generated by a series circuit consisting of a pulse generator (clock), a counter counting the pulses and a digital to analog converter, converting the counter output into a dc signal. As soon as V_c is equal to V_i, the input comparator closes a gate between the clock and the counter, the counter stops and its output is shown on the display.

Operation of the Circuit:-

The clock generates pulses continuously. At the start of a measurement, the counter is reset to 0 at time $t_1$so that the output of the digital to analog converter (DAC) is also 0. If V_i is not equal to zero, the input comparator applies an output voltage that opens the gate so that clock pulses are passed on to the counter through the gate. The counter starts counting and the DAC starts to produce an output voltage increasing by one small step at each count of the counter. The result is a staircase voltage applied to the second input of the comparator, as shown in Fig. 5.9.

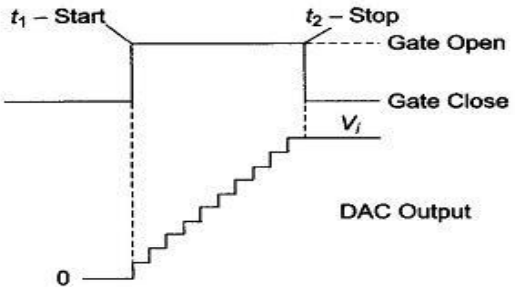


Fig.5.28: Staircase Waveform

This process continues until the staircase voltage is equal to or slightly greater than the input voltage V_i. At that instant t_2, the output voltage of the input comparator changes state or polarity, so that the gate closes and the counter is stopped.

The display unit shows the result of the count. As each count corresponds to a constant dc step in the DAC output voltage, the number of counts is directly proportional to V_c and hence to V_i. By

appropriate choice of reference voltage, the step height of the staircase voltage can be determined. For example, each count can represent 1 mV and direct reading of the input voltage in volts can be realized by placing a decimal point in front of the 10 decade.

Basic concept of D/A converters

Digital to analog Converter:-A **Digital to Analog Converter (DAC)** converts a digital input signal into an analog output signal. The digital signal is represented with a binary code, which is a combination of bits 0 and 1. This chapter deals with Digital to Analog Converters in detail. The **block diagram** of DAC is shown in the following figure 5.29:-

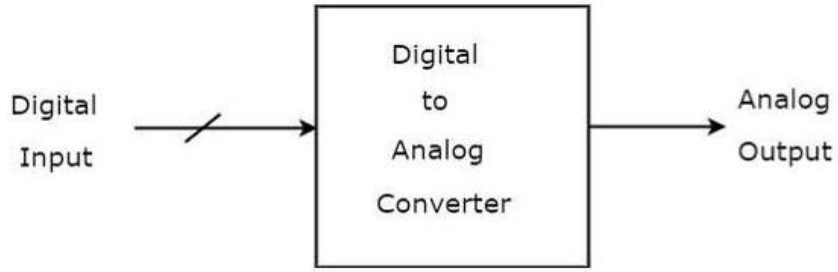


Fig.5.29: block diagram of DAC

A Digital to Analog Converter (DAC) consists of a number of binary inputs and a single output. In general, the **number of binary inputs** of a DAC will be a power of two.

Types of DACs

There are **two types** of DACs

- Weighted Resistor DAC
- R-2R Ladder DAC

This section discusses about these two types of DACs in detail –

Weighted Resistor DAC

A weighted resistor DAC produces an analog output, which is almost equal to the digital (binary) input by using **binary weighted resistors** in the inverting adder circuit. In short, a binary weighted resistor DAC is called as weighted resistor DAC.

The **circuit diagram** of a 3-bit binary weighted resistor DAC is shown in the following fig.5.30

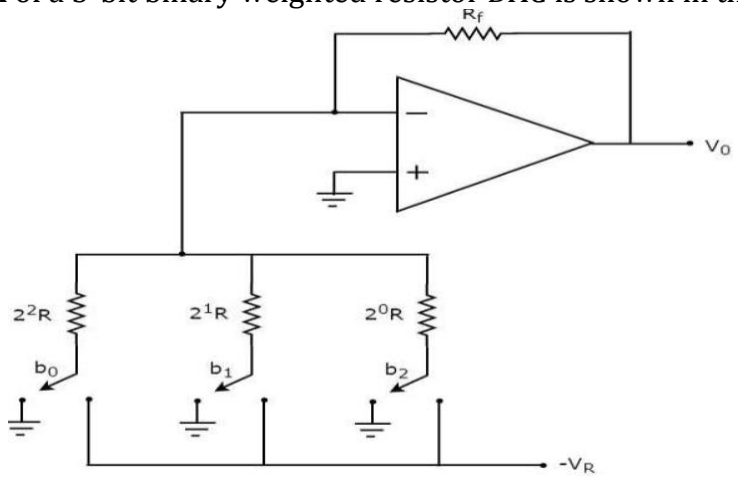


Fig.5.30: circuit diagram of a 3-bit binary weighted resistor DAC

Recall that the bits of a binary number can have only one of the two values. i.e.,either 0 or 1. Let the **3-bit binary input** is $b_2b_1b_0b_2b_1b_0$. Here, the bits b_2b_2 and b_0b_0 denote the **Most Significant Bit (MSB) and Least Significant Bit (LSB)** respectively.

The **digital switches** shown in the above figure will be connected to ground, when the corresponding input bits are equal to '0'. Similarly, the digital switches shown in the above figure will be connected to the negative reference voltage, $-V_R-V_R$ when the corresponding input bits are equal to '1'.In the above circuit, the non-inverting input terminal of an op-amp is connected to ground. That means zero volts is applied at the non-inverting input terminal of op-amp. According to the **virtual short concept**, the voltage at the inverting input terminal of opamp is same as that of the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal's node will be zero volts.

Binary Weighted Resistor DAC:-

In the weighted resistor type DAC, each digital level is converted into an equivalent analog voltage or current. The following figure shows the circuit diagram of the binary weighted resistor type DAC.

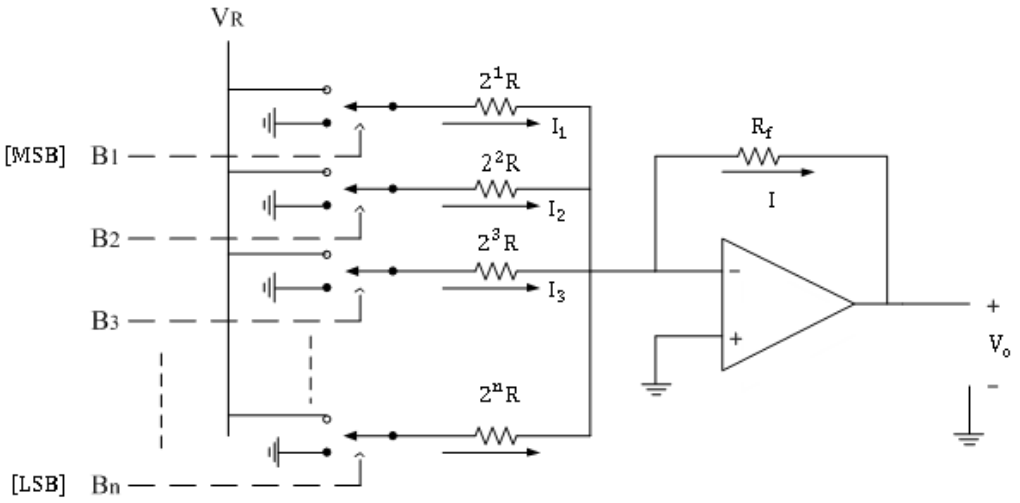


Fig.:5.31: Binary Weighted Resistor DAC

It consists of parallel binary weighted resistor bank and a feedback resistor Rf. The switch positions decides the binary word (i.e. B_1 $B_2B_3...B_n$). In the circuit op-amp is used as current to voltage converter.

Analysis:

Let us analyze the circuit using normal analysis concepts used in op-amp. When the switches are closed the respective currents are flowing through resistors as shown in the circuit diagram above.

Since input current to the op-amp is zero, the addition current flows through feedback resistor.

$\therefore I=I_1+I_2+I_3+$ ……$+I_n$

The inverting terminal of op-amp is virtually at ground potential.

Disadvantages:

1) When number of binary input increases, it is not easy to maintain the resistance ratio.

2) Very wide ranges of different values of resistors are required. For high accuracy of conversion, the values of resistances must be accurate.

3) Different current flows through resistors, so their wattage ratings are also different.
4) Accuracy and stability of conversion depends primarily on the absolute accuracy of the resistors and tracking of each other with temperature. eg. For 10 digit converter small resistance value = 10 kΩ and large resistance value = 5.12 MΩ It is very difficult and expensive to obtain stable precise resistances of such value.
5) Since 'R' is very large, op-amp bias currents gives a drop which offsets output.
6) Resistances of switches may be comparable with smallest resistor.

R-2R Ladder DAC:-

The following circuit diagram shows the basic 2 bit R-2R ladder DAC circuit using op-amp. Here only two values of resistors are required i.e. R and 2R. The number of digits per binary word is assumed to be two (i.e. n = 2). The switch positions decides the binary word (i.e. B1 B0)

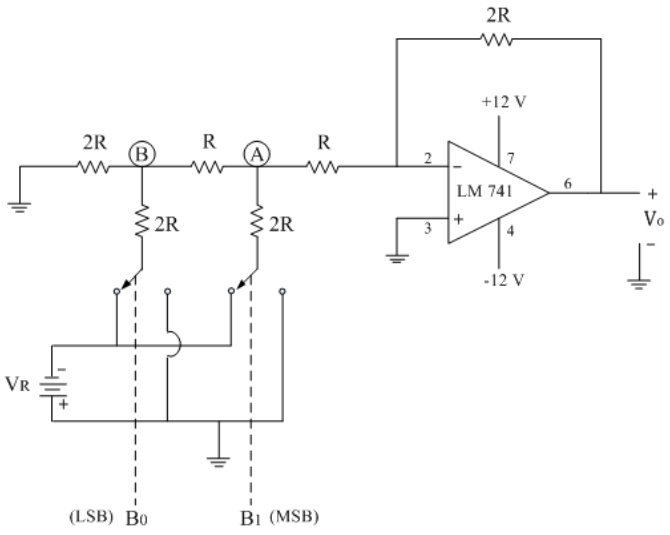


Fig.5.32: R-2R Ladder DAC

The typical value of feedback resistor is Rf = 2R. The resistance R is normally selected any value between 2.5 kΩ to 10 kΩ.

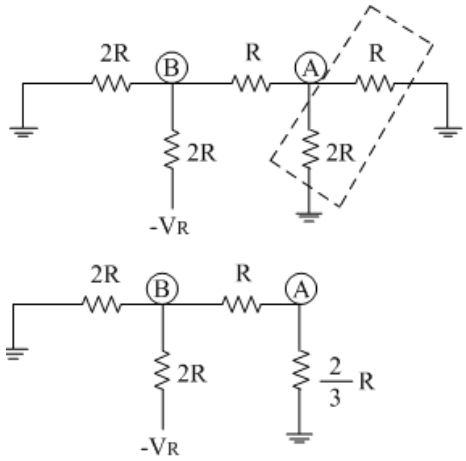
The generalized analog output voltage equation can be given as

$$V_o = -V_R \frac{R_f}{R}\left[\frac{B_1}{2^1}+\frac{B_2}{2^2}+\frac{B_3}{2^3}+----+\frac{B_n}{2^n}\right]$$

$$\therefore V_o = -V_R \frac{R_f}{R\times 2^n}[B_1 2^{n-1}+B_2 2^{n-2}+B_3 2^{n-3}+--+B_n 2^{n-n}]$$

$$\therefore V_o = -V_R \frac{R_f}{R\times 2^n}[B_1 2^{n-1}+B_2 2^{n-2}+B_3 2^{n-3}+--+B_n 2^{0}]$$

The operation of the above ladder type DAC is explained with the binary word (B1B0= 01) The above circuit can be drawn as,



Applying the nodal analysis concept at point (A), we gets following equations

$$\frac{V_A}{\frac{2}{3}R}+\frac{V_A-V_B}{R}=0$$

$$\therefore \frac{3V_A}{2R}+\frac{V_A-V_B}{R}=0$$

$$\therefore \frac{3V_A+2V_A-2V_B}{2R}=0$$

$$\therefore\ 5V_A=2V_B$$

$$\therefore\ V_B=\frac{5V_A}{2}$$

The voltage at point A i.e. V_A is applied as input to the op-amp which is in inverting amplifier mode as shown in figure below.

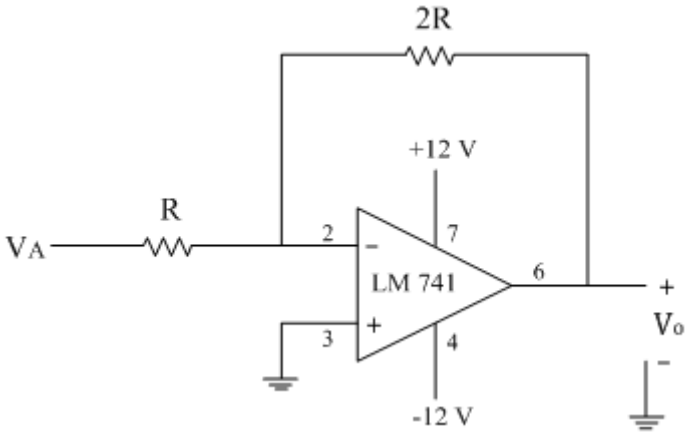


Fig.5.33: Inverting amplifier op-amp

The output voltage of the complete setup $\therefore V_o=-(2R/R)\ V_A$

$\therefore V_o=-(2R/R)(-V*R/8)$

$\therefore V_o=V*R/4$

Similarly for other three combinations of digital input the analog output voltage V_o is calculated as follows

Sr. No.	Digital Input		Analog Output, V_o(V)
	B_1	B_0	
01	0	0	0
02	0	1	$\frac{V_R}{4}$
03	1	0	$\frac{2V_R}{4}$
04	1	1	$\frac{3V_R}{4}$

Applications

ADC applications	DAC applications
1. Digital Voltmeter: measures voltage in analog and convert to digital form using ADC for digital representation form.	1. Modems need DAC to convert data to analog form so that it can be carried over telephone wires.
2. Mobile phone: Analog voice is converted to digital form for further processing(speech compression, encoding etc.) before it is converted back to analog form for transmission.	2. Video adapters also need DACs known as RAMDACs to convert digital form of data to analog form.
3. Scanner: When we take photo, the scanner uses ADC internally to convert analog information provided by picture into digital information.	3. Digital Motor Control
4. Voice Recorder: It uses ADC to convert analog voice information to the digital information. Latest VOIP solutions utilize the same concept.	4. Printers

EXERCISE UNIT – 5

OBJECTIVE TYPE QUESTION

SECTION –A

Multiple Choice Questions:

Q. 1 A MUX means

(a) many into one device (b) one into many device

(c) many into many device (d) None

Q. 2 In a MUX, the input data lines N and select input data lines m are given

by a relation :

(a) $m= 2^N$ (b) $2^m=N$

(c) m= 2N (d) N= 2m

Q. 3 A 8:1 MUX has ... select lines

(a) 4 (b) 3

(c) 8 (d) 2

Q. 4 A 32:1 MUX has..... select lines

(a) 6 (b) 8

(c)5 (d) 7

Q. 5 A multiplexer is used for

(a) Serial to parallel data conversion (b) Parallel to serial data conversion

(c) Serial to serial data conversion (d) Parallel to parallel data conversion

Q. 6 How many output data lines are there in a 32:1 multiplexer?

(a) 1 (b) 82

(c) 8 (d) None

Q. 7 A demultiplexer can be used as

(a) Encoder (b) Decoder

(c) LCD device (d) None

Q. 8 A Demux performs the reverse operation of

(a)Encoder (b) Decoder

(c) MUX (d) None

Q. 9 A1: 32 Demux has .. output data lines

(a) 32 (b) 1

(c) 16 (d) None

Q. 10 A Demux can be used for

(a) Parallel to serial data conversion (b) Serial to parallel data conversion

(c) Parallel to parallel data conversion (d) None

Q. 11 IC 74151 is a

(a) 4:1 Mux (b) 8:1 Mux

(c) 1:4 Demux (d) 1:8 Demux

Q. 12. D flip-flop is...flip-flop

(a) Digital (b) Differential

(c) Delayed (d) Dial type

Q. 13 ..... flip-flop does not have race around condition

(a) Master slave (b) D flip-flop

(c) RS flip-flop (d) J-K flip-flop

Q. 14 If both input of SR flip-flop is high the, flip-flop respond to

(a) Set mode (b) Reset mode

(c) No change (d) Invalid mode

Q. 15 Flip-flop and latch belong to the following logic circuit known as
(a) Bistable multivibrator (b) Astable multivibrator
(c) Schemitt trigger (d) Monostable multivibrator

Q. 16 If both input of J-K flip-flop is high then the flip-flop respond to
(a) Set mode (b) Reset mode
(c)Toggle mode (d) No change

Q. 17 For J=0, K= 0, the flip-flop respond to
(a) Set mode (b) Reset mode
(c)Toggle mode (d) No change mode

Q. 18 For J = 0, K = 1, the flip-flop respond to
(a)Reset mode (b) Set mode
(c) No change mode (d) Toggle mode

Q. 19 For J = 1, K = 0, the flip-flop respond to
(a)Reset mode (b) Set mode
(c) Toggle mode (d) No change mode

Q. 20 For D = 0 flip-flop respond to
(a) Set (b) Reset
(c) No change (d) Toggle

Q. 21 A flip-flop is used as latch
(a) T (b) J-K
(c) Master slave J-K flip-flop (d) RS flip-flop

Q. 22 A half adder is characterized by:
(a) Three inputs and two outputs (b) Two inputs and two outputs
(c) Two inputs ad one output (d) Two inputs and three outputs

Q. 23 A full adder is characterized by:
(a) Three inputs and three outputs (b) Three inputs and four outputs
(c) Three inputs and two output (d) None

Q. 24 The inputs to a full adder are A = 1, B = 1 and C = 1. The outputs are
(a) S=1, Co = 1 (b) S= 0, Co = 1
(c)S=1, Co=0 (d) None

Q. 25 A full adder can add .... bits
(a) 2 (b) 4
(c)3 (d) 5

Q. 26 Which logic circuit has a memory
(a) Combinational logic circuit (b)Sequential logic circuit
(c) Both (d) None

SHORT TYPE QUESTION

SECTION – B

Q. 1 Explain the term multiplexer. Design a 2 :1 multiplexer.
Q. 2. Give the block diagrams, truth table and logic circuit for a 4: 1 MUX.
Q. 3 Design the following multiplexers
(i) 8:1 MUX
(ii) 16: 1 MUX
Q. 4. How can you design a 32:1 multiplexer by using 16:1 MUX and 2:1 MUX?
Q. 5 What do you mean by multiplexer tree?
Q. 6 Can a multiplexer be used for realizing a logic function?
Q. 7 What is the function of select lines in a MUX?
Q. 8 What are the applications of a MUX?
Q. 9 What do you mean by demultiplexer?
Q. 10 Design a 1: 4 and 1:8 DEMUX.
Q. 11 What is the difference between MUX and DEMUX?
Q. 12 Write a short note on
(i) Combinational circuit
(ii) Sequential circuit.
Q. 13 What is the major difference between the sequential circuit and combinational circuit?
Q. 14 Write the truth table, logical expression and logic diagram of a half adder.
Q. 15 Write about the truth table, logic diagram of a full adder.
Q. 16 How many types of logic circuits are these?
Q. 17 Define Flip flop?
Q. 18 What is the mode of SR flip-flop when inputs of SR flip-flop are high?.
Q. 19 What is the mode of J-K flip-flop when inputs of J-K flip-flop are High?
Q. 20 Give two applications of flip-flop.
Q. 21 Explain how JK flip-flop can work as T flip-flop

LONG TYPE QUESTION

SECTION – C

Q. 1 What do you mean by a MUX? Design a 32:1 MUX by using 16: 1 MUX and 2:1 MUX?
Q. 2 Explain with the help of block diagram, truth table, Boolean expression and logic circuit of a 16: 1 MUX.
Q. 3 What do you mean by DEMUX? Design a 1:8 DEMUX by using truth table, logical expression and logic circuit.
Q. 4 What is difference between flip-flop and latch?
Q. 5 Draw the truth table of RS latch and also explain its working using NAND gate.
Q. 6 How you will obtain D latch using SR latch and explain the truth table of D flip-flop?
Q. 7 What is the drawback of J-K flip-flop and how it will be removed?
Q. 8 What do you understand by Race around condition of the flip-flop?
Q. 9 Explain the working of master slave J-K flip-flop and it will overcome the race around condition of the flip-flop.
Q. 10 Explain the working of T flip-flop.
Q. 11 Explain the operation of negative edge triggered SR flip-flop.

Q. 12 What are the drawbacks of SR flip-flop? How it will be overcome?
Q. 13 Explain the operation of J-K flip-flop using NAND gate.

Answer of section A

1. (a)	2. (b)	3. (b)	4. (c)	5. (b)	6. (a)
7. (b)	8. (c)	9. (a)	10. (b)	11. (b)	12. (c)
13. (a)	14. (d)	15. (a)	16. (c)	17. (d)	18. (a)
19. (b)	20. (b)	21. (d)	22. (b)	23. (c)	24. (a)
25. (c)	26. (b)				

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